Ultra-low-Power Networked Systems

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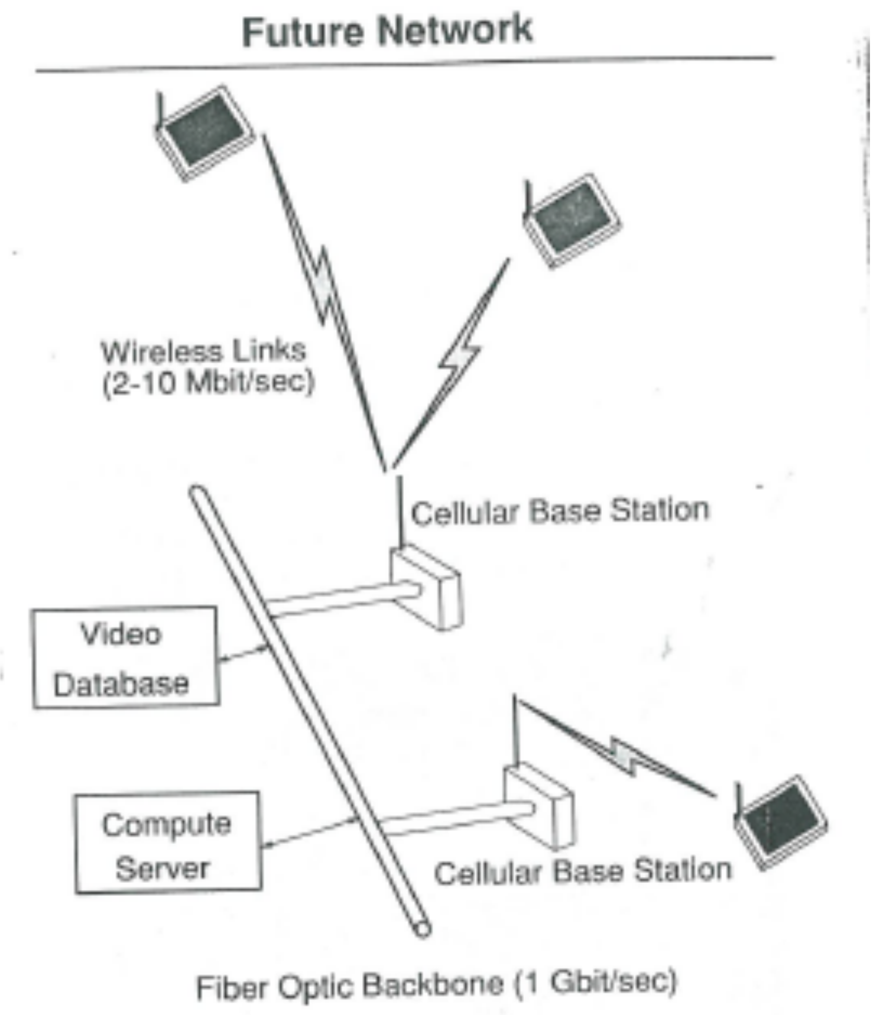
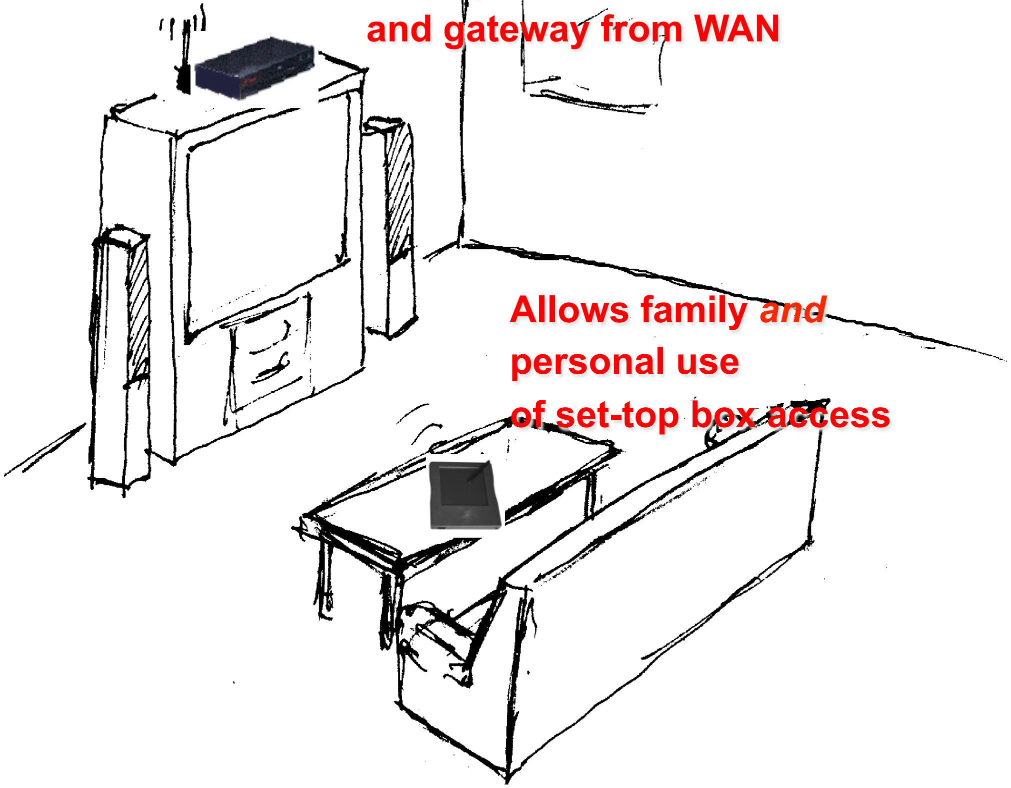
MIT EECS ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

Wireless Vision: 1990





Set-top box doubles as basestation
and gateway from WAN

Allows family *and*
personal use
of set-top box access

1990 WINLAB workshop on Third
Generation Wireless Information Networks

Prof. R. Brodersen, BWRC

The InfoPad Project – rewind 20 years

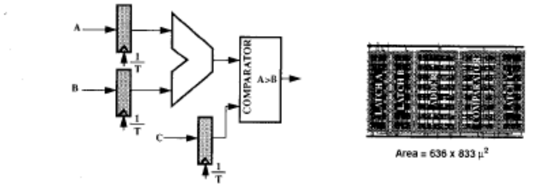


Fig. 7. A simple data path with corresponding layout.

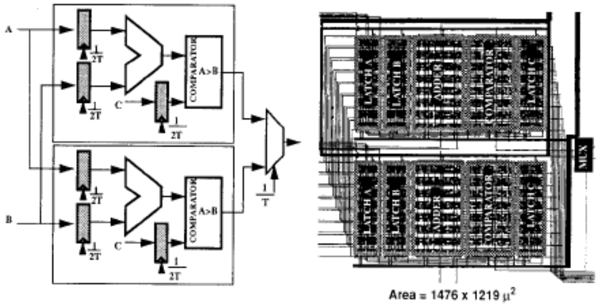


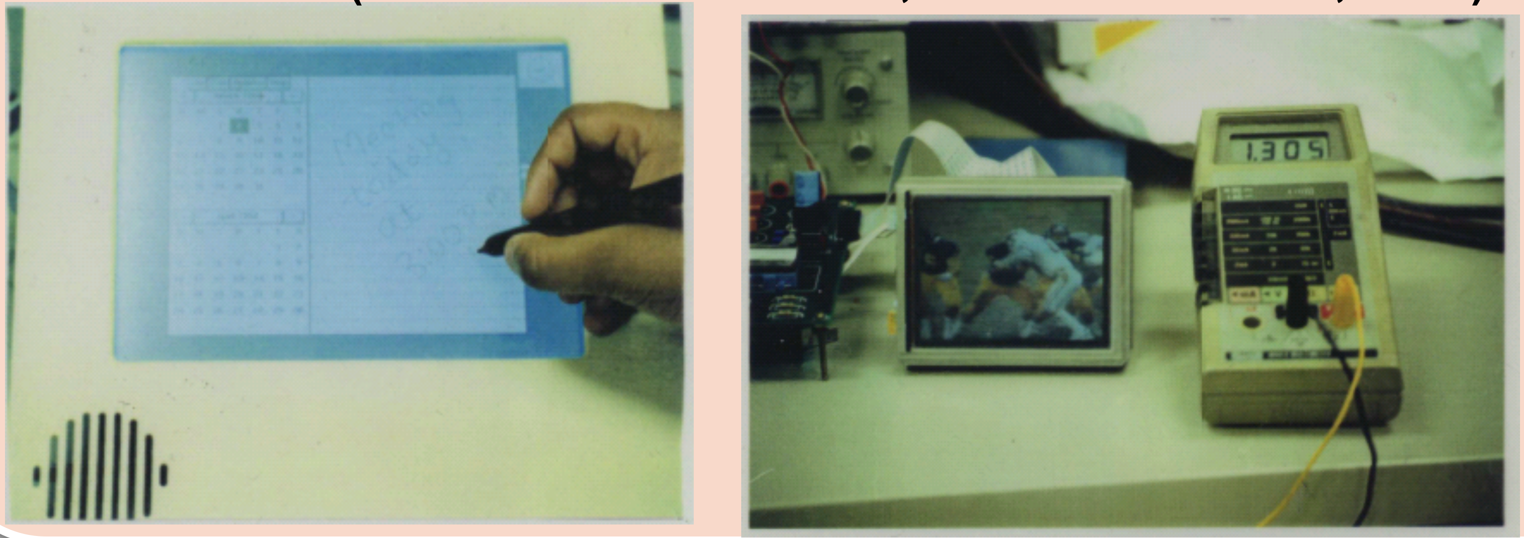
Fig. 8. Parallel implementation of the simple data path.

Parallelism = Energy Efficiency

A. Chandrakasan, S. Sheng, R. Brodersen, "Low-power Digital CMOS Design" (April 1992)

"slower is better"

The InfoPad (Anantha Chandrakasan, Robert Brodersen, et al.) – ISSCC 1994

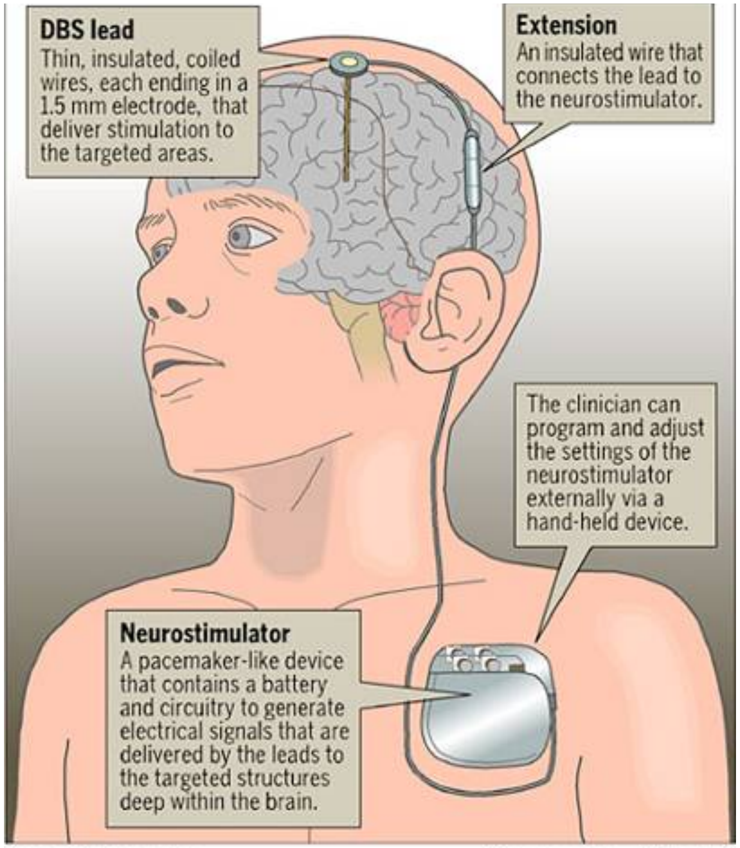


6 ICs < 2mW

Research ICs: mW (1990) ⇨µW (current) ⇨nW (future)

Energy Efficiency is Still a Key Consideration

Deep Brain Stimulator



DBS lead
Thin, insulated, coiled wires, each ending in a 1.5 mm electrode, that deliver stimulation to the targeted areas.

Extension
An insulated wire that connects the lead to the neurostimulator.

The clinician can program and adjust the settings of the neurostimulator externally via a hand-held device.

Neurostimulator
A pacemaker-like device that contains a battery and circuitry to generate electrical signals that are delivered by the leads to the targeted structures deep within the brain.

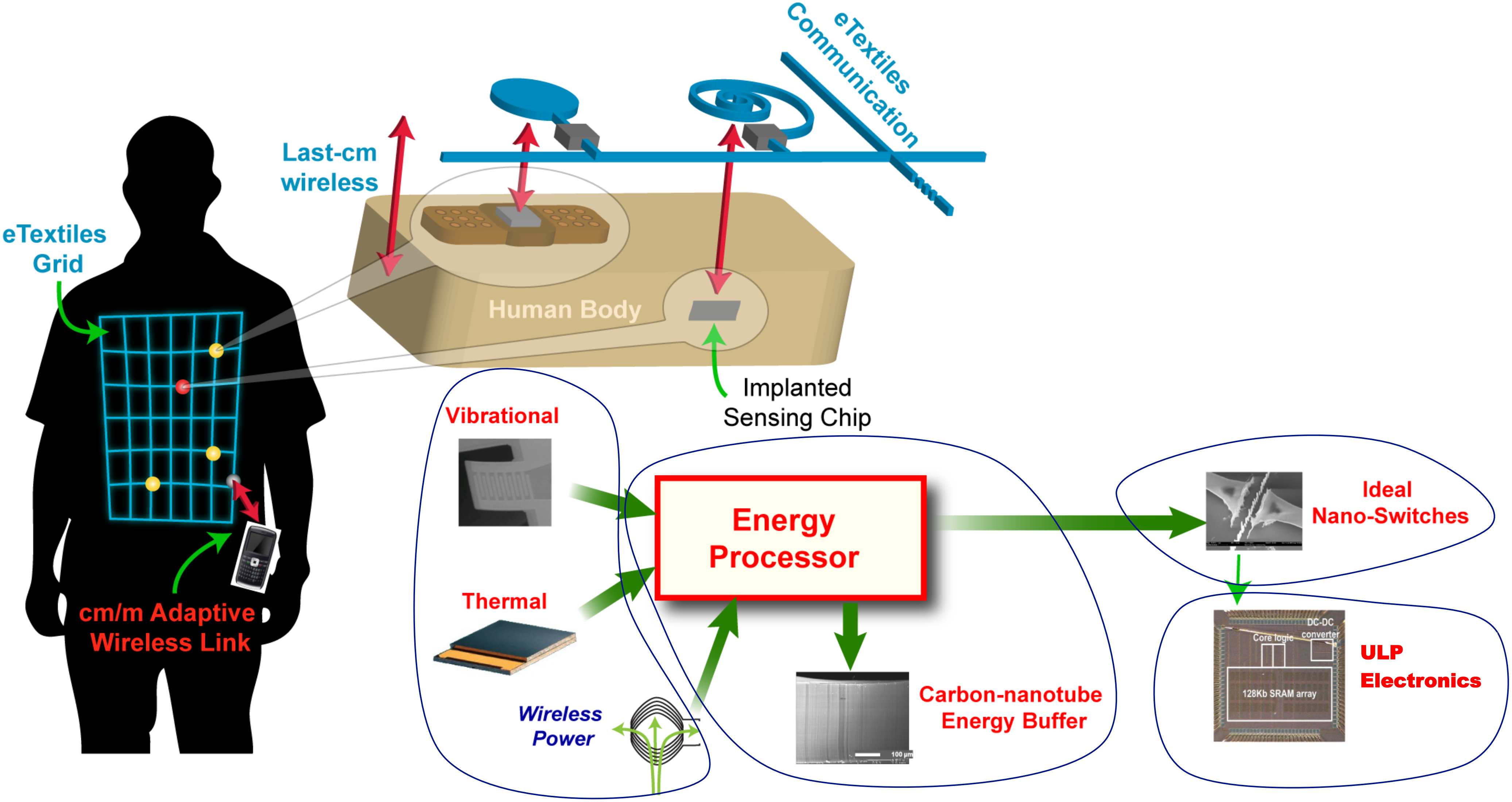
Source: Medtronic Inc. **Steve Greenberg / Star staff**

Courtesy of Tim Denison (Medtronic)

Battery lasts about 5 years - surgery needed to replace it!

Energy Efficiency Impacts Time Between Surgery

Self-Powered Connected Personal Health



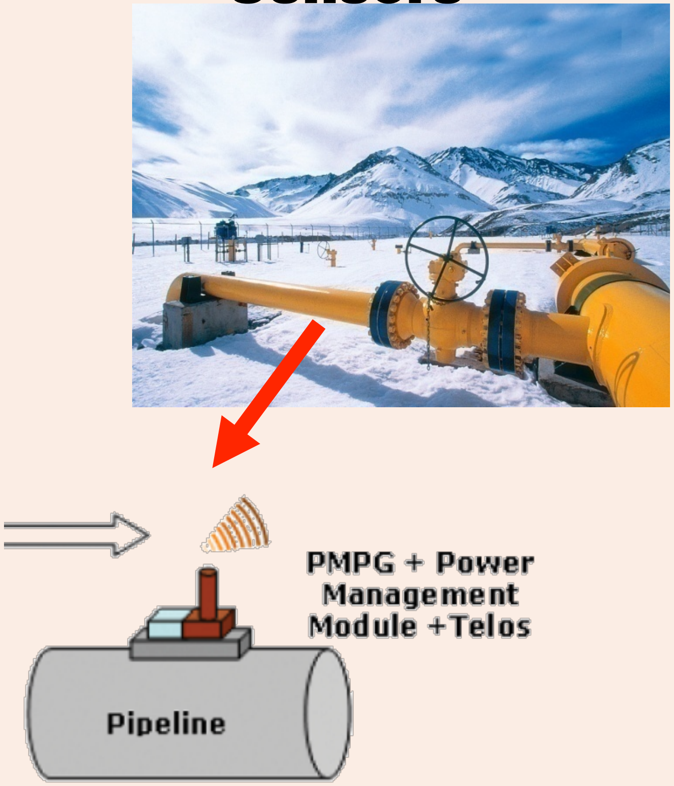
Enable a New Class of Bio-Medical Systems that Leverage the Power of Silicon and Nanotechnology

Key Enablers of Internet of Everything

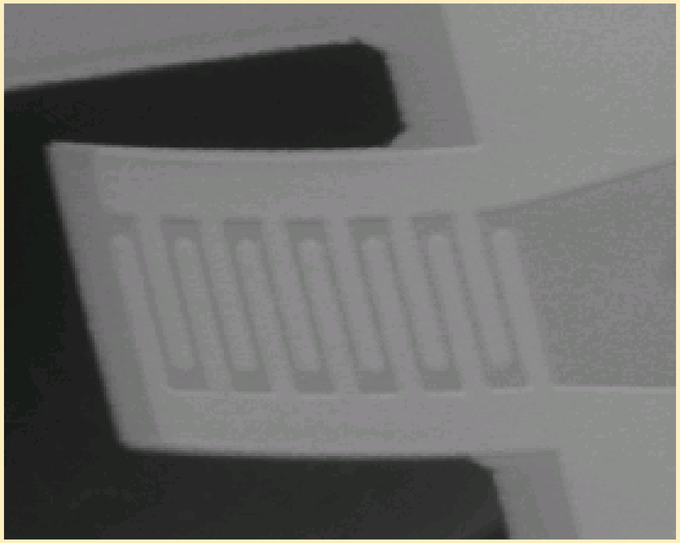
- Tremendous advances in <u>commercial</u> low-power electronics – ultra-low-power sensors, radios, signal processing, energy harvesting
- Cost reduction of electronic components
- Simple interfaces – easy access through smartphone apps (medical, fitness, energy, etc.)
- Standards for internet-of-things
- Compelling applications that matter to the end users – e.g., fitbit and fitness monitors

Vibration-to-Electric Energy

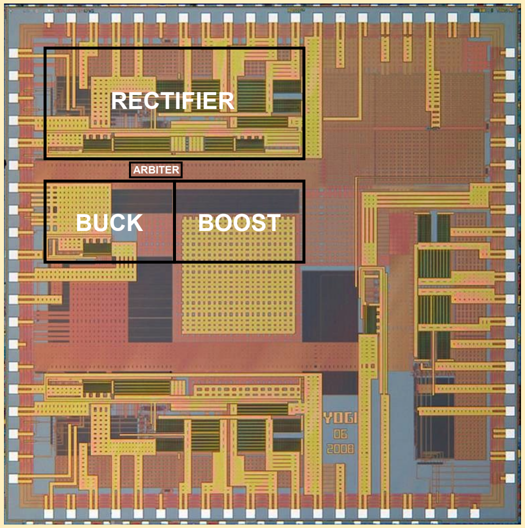
Self-powered Wireless Corrosion Monitoring Sensors



Piezoelectric Micro-Power Generators



Power Converter



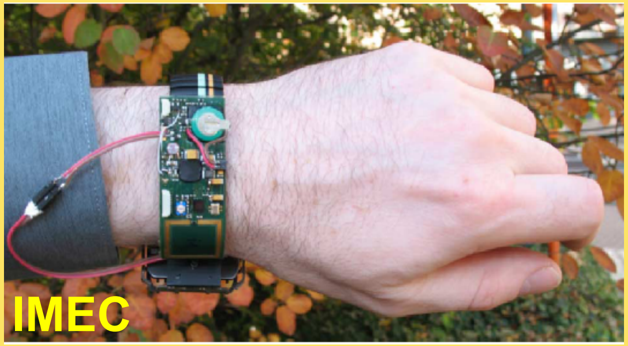
Sang-Gook Kim (MIT)

10μW -100μW generated

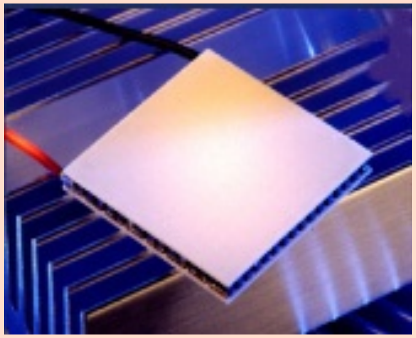
Vibrations Power Distributed Sensor Devices (Battery-less Operation)

Body Heat Powered Electronics

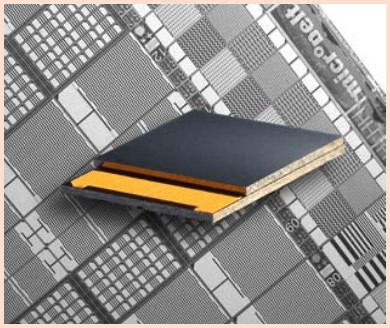
System Concept



Thermo-Electric Devices

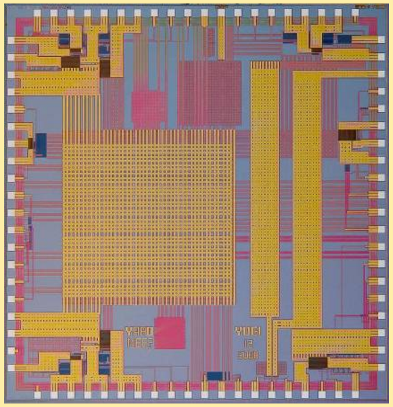


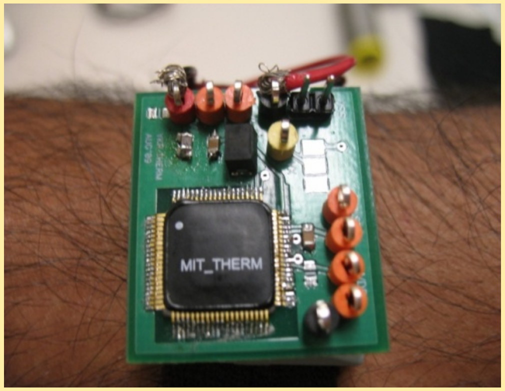
Tellurex



Micro-pelt

Thermal Energy Chip

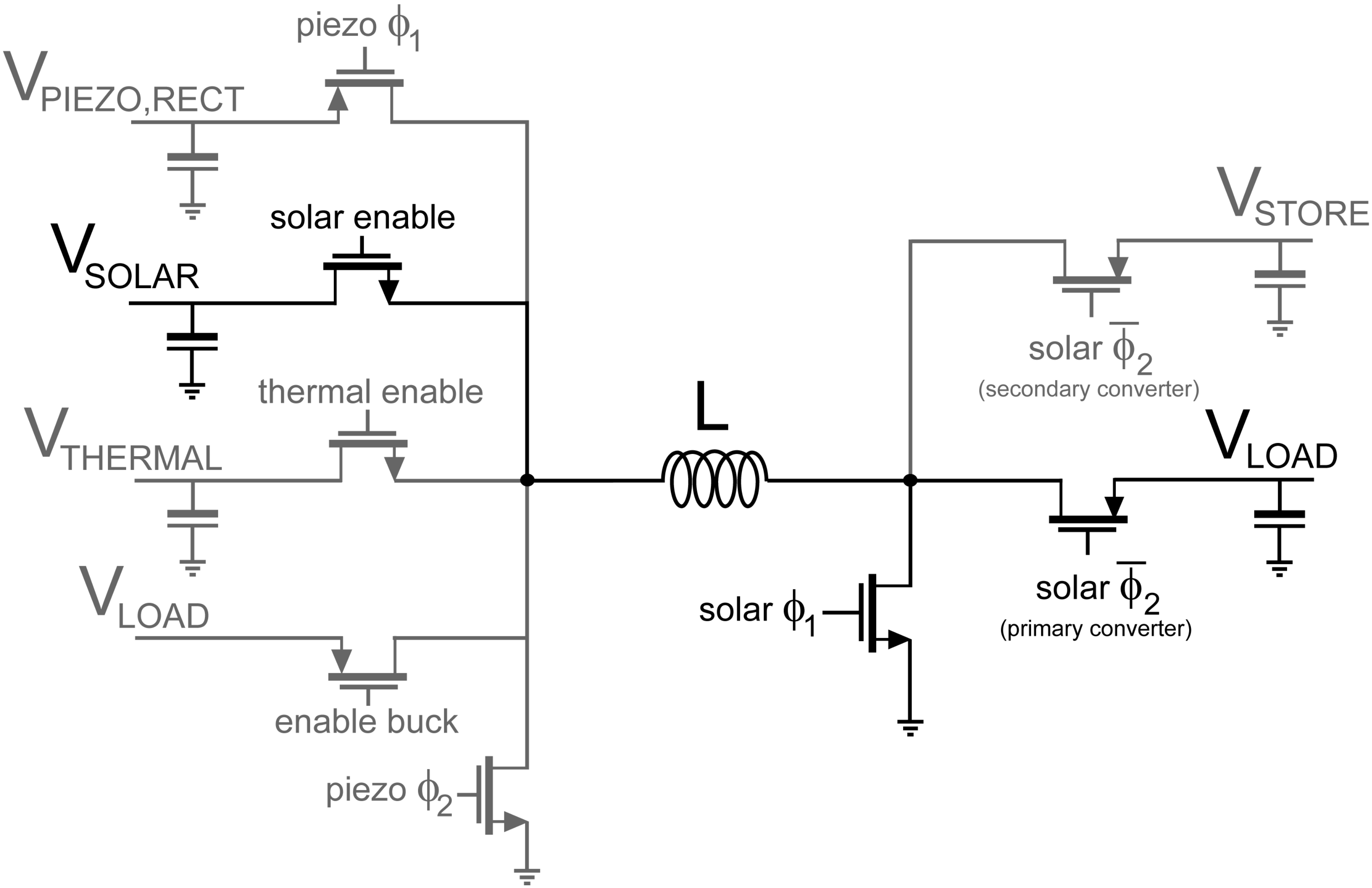




[Y. Ramadass and A. Chandrakasan, ISSCC 2010]

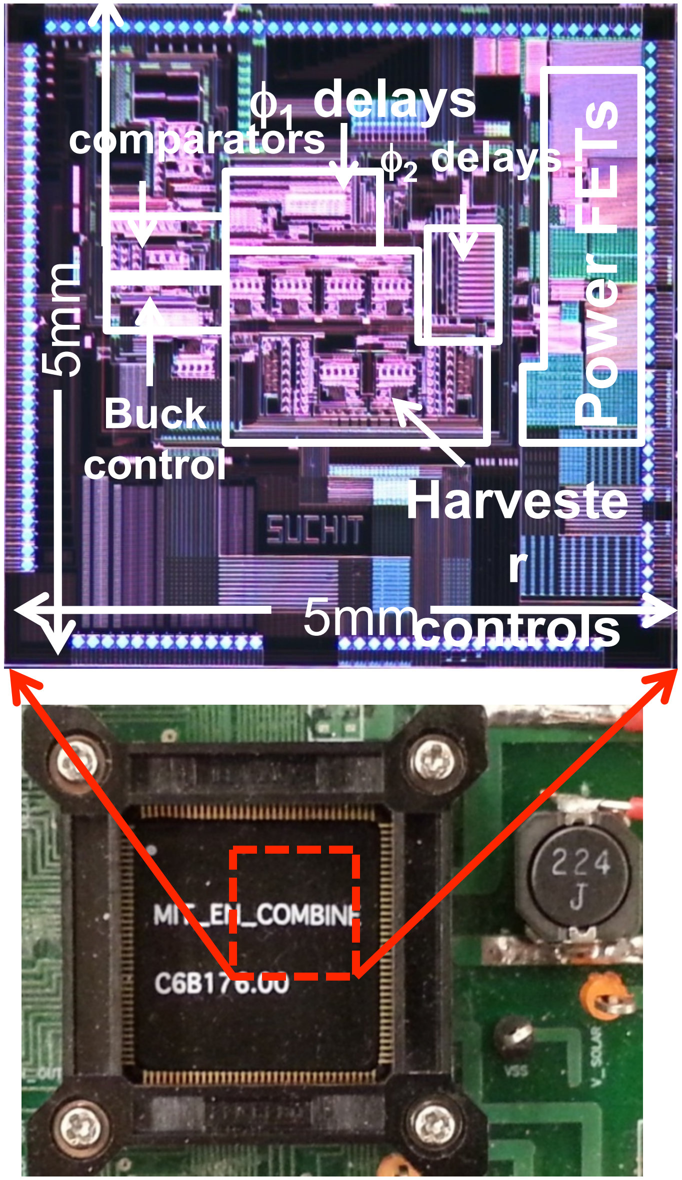
Future ULP Electronics (e.g., body worn sensors) Can be Powered from Body Heat

Energy Combining : Solar, Thermal, Vibrations



- **Shared inductor minimizes board components**

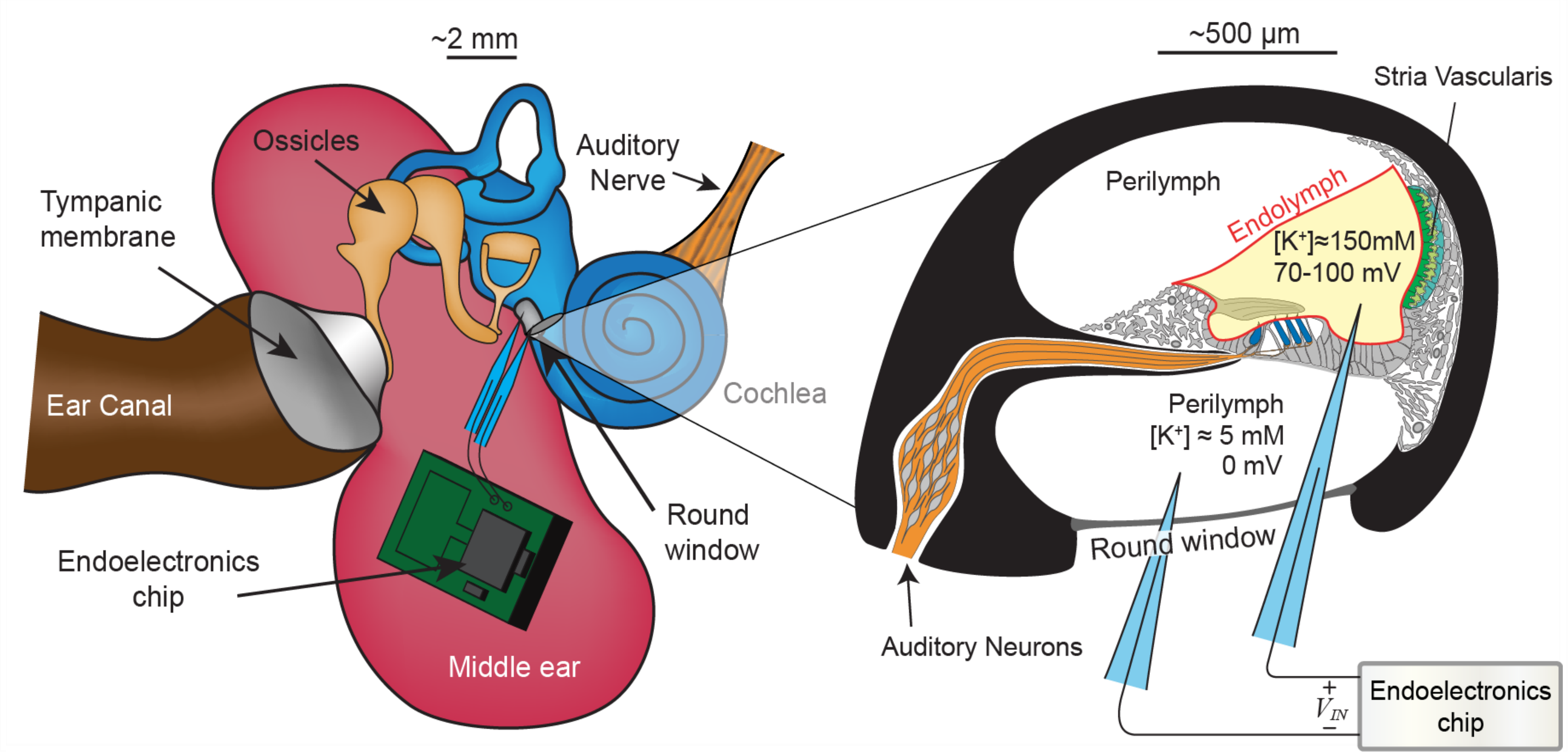
Multi-Input Energy Harvesting Design Summary



Technology	0.35μm CMOS
Input Voltages	20 - 150mV Thermal 0.2 - 0.75V Solar 1.5 – 5V Piezoelectric
Output Voltages	1.8V Regulated 1.8 - 3.3V Storage
Passives	1 Inductor (22μH) 5 capacitors
Thermal: Seebeck 50mV/K, ΔT=1.7K **Solar:** 1500lux, 15cm^2 **Piezoelectric:** PZT 3in^2, 1g	**Thermal Boost:** 96μW **Solar Boost:** 262μW **Piezoelectric Buck-Boost:** 40μW **Total Power:** 398μW

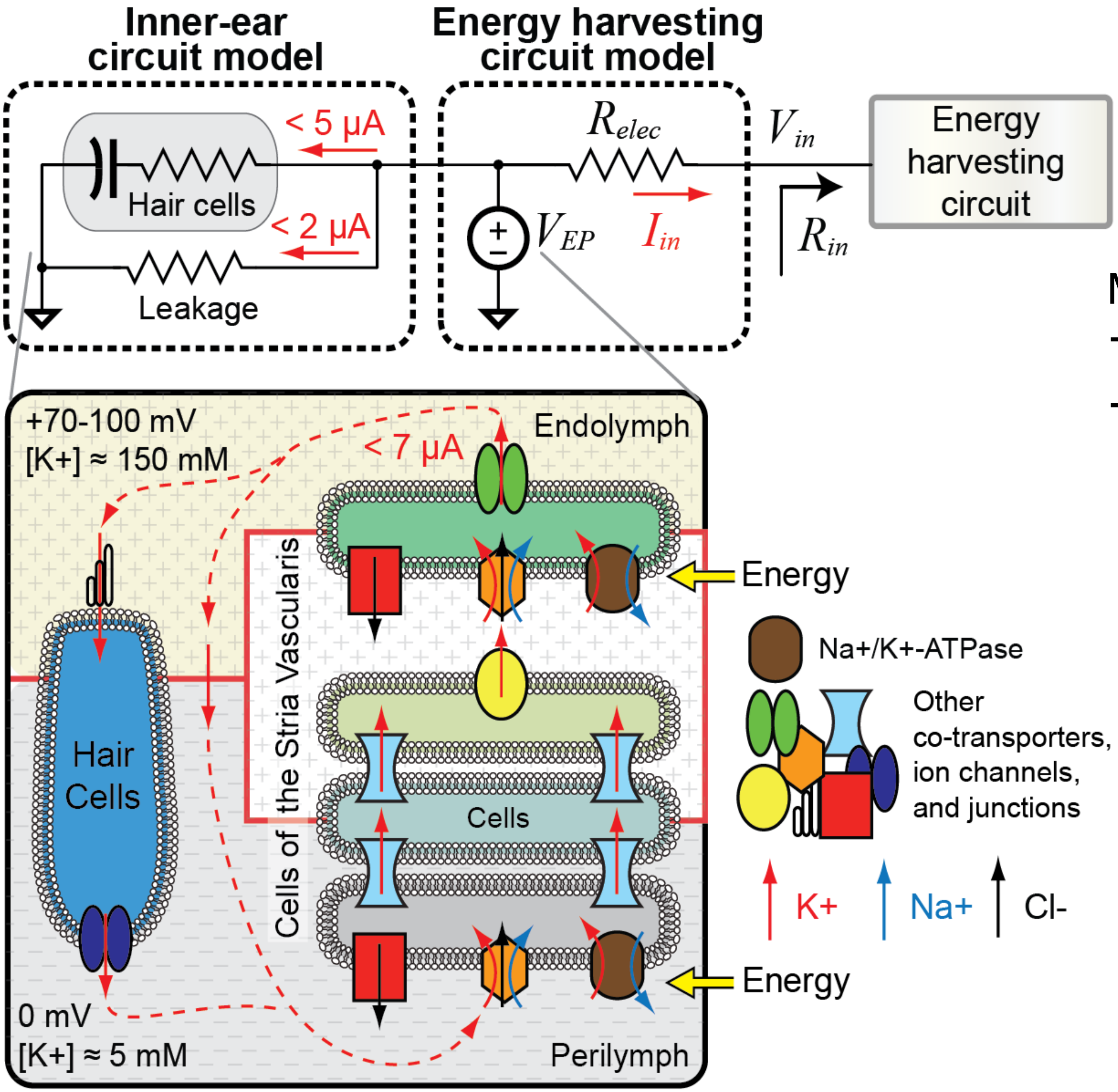
[Bandyopadhyay, JSSC 2012]

A (New) energy harvesting source: inside the inner-ear



Can we tap the energy reservoir in the ***endocochlear potential*** to power electronics?

Endocochlear Potential circuit model

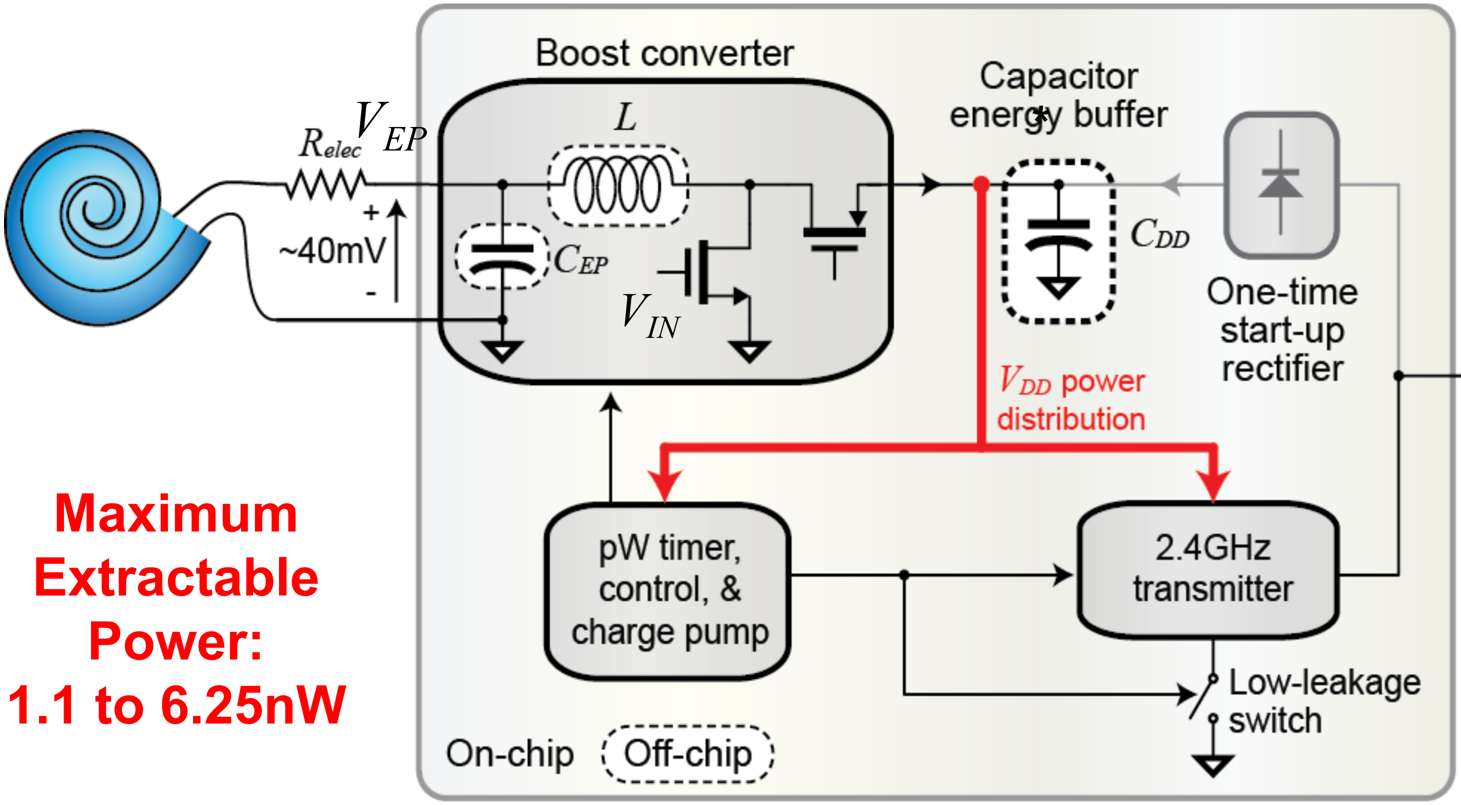


Maximum energy extraction
→ maximum power transfer
→ Set $R_{in} = R_{elec}$

$$P_{EP,\max} = \left(\frac{V_{EP}}{2}\right)^2 \frac{1}{R_{in}}$$

$$= \frac{(40\mathrm{mV})^2}{1\mathrm{M\Omega}} = 1.6\mathrm{nW}$$

Endoelectronics chip:
EP harvester architecture



Maximum Extractable Power: 1.1 to 6.25nW


nature biotechnology

VOLUME 30 NUMBER 12 DECEMBER 2012

Battery power from the inner ear
mRNA influenza vaccine
Single-molecule methyl sequencing

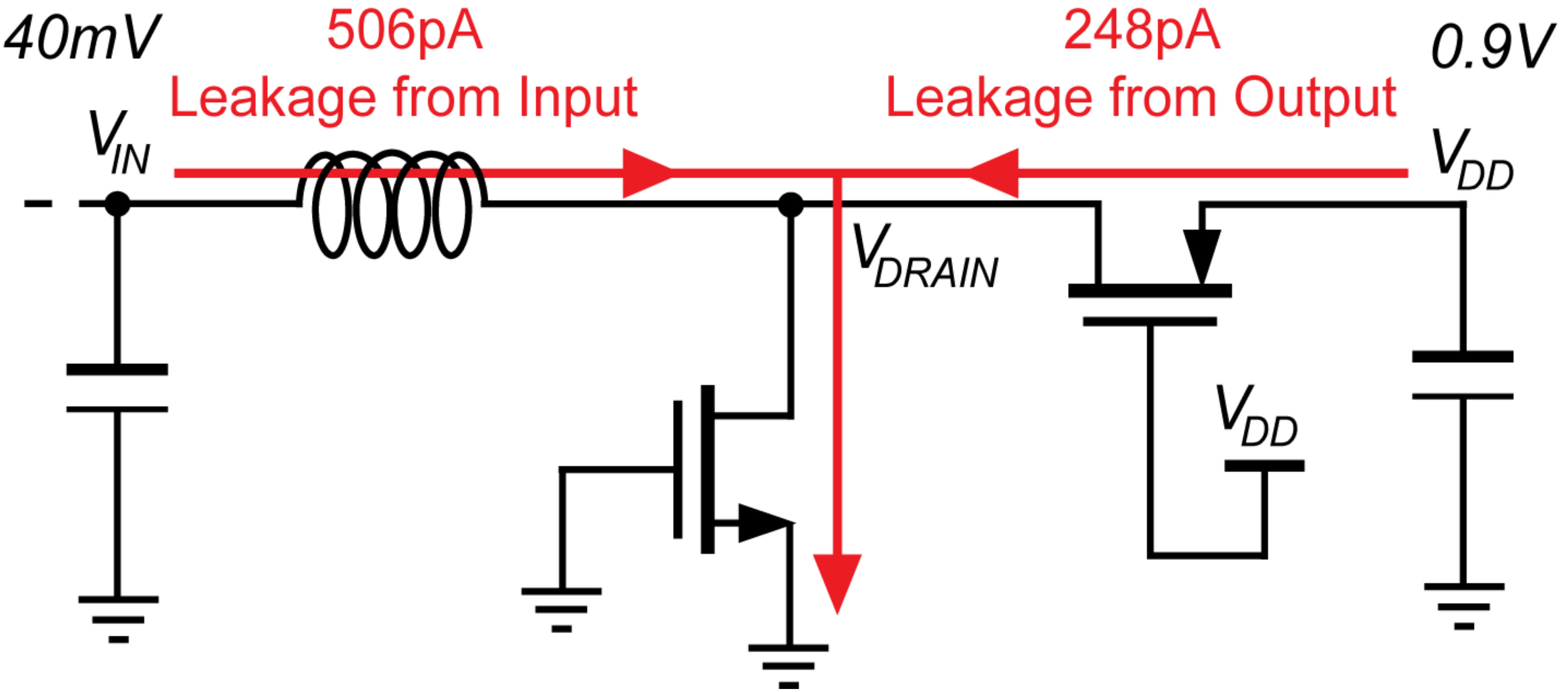
The endocochlear potential (EP) was discovered 60 years ago by Georg von Békésy

In 1961, he won a Nobel Prize for his work on the ear

The EP has never before been used as an energy source for electronics

With S. Bandyopadhyay, A. Lysaght, P. Mercier, Dr. K. Stankovic

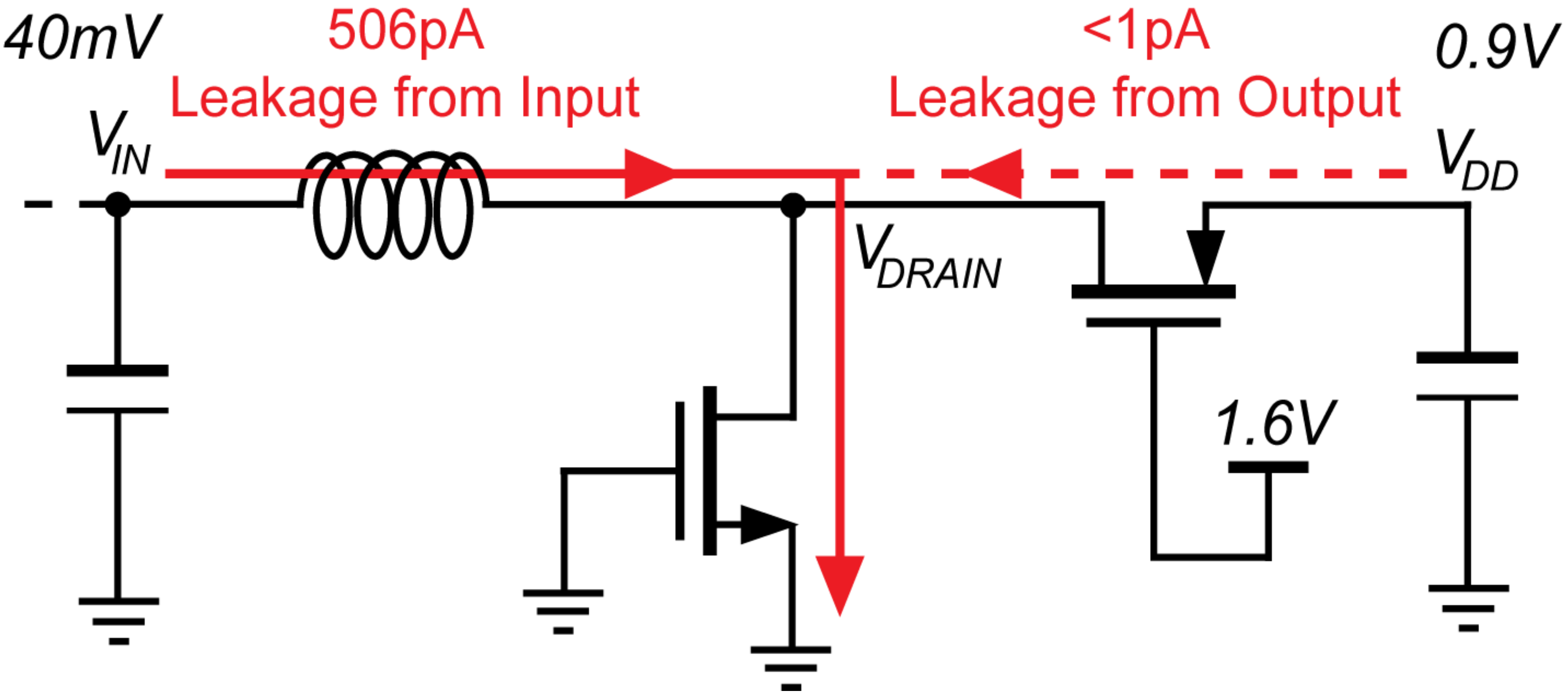
Every Picowatt Counts!



Leakage Power
from Input: 20pW

Leakage Power
from Output: 223pW

Every Picowatt Counts!



Leakage Power
from Input: 20pW

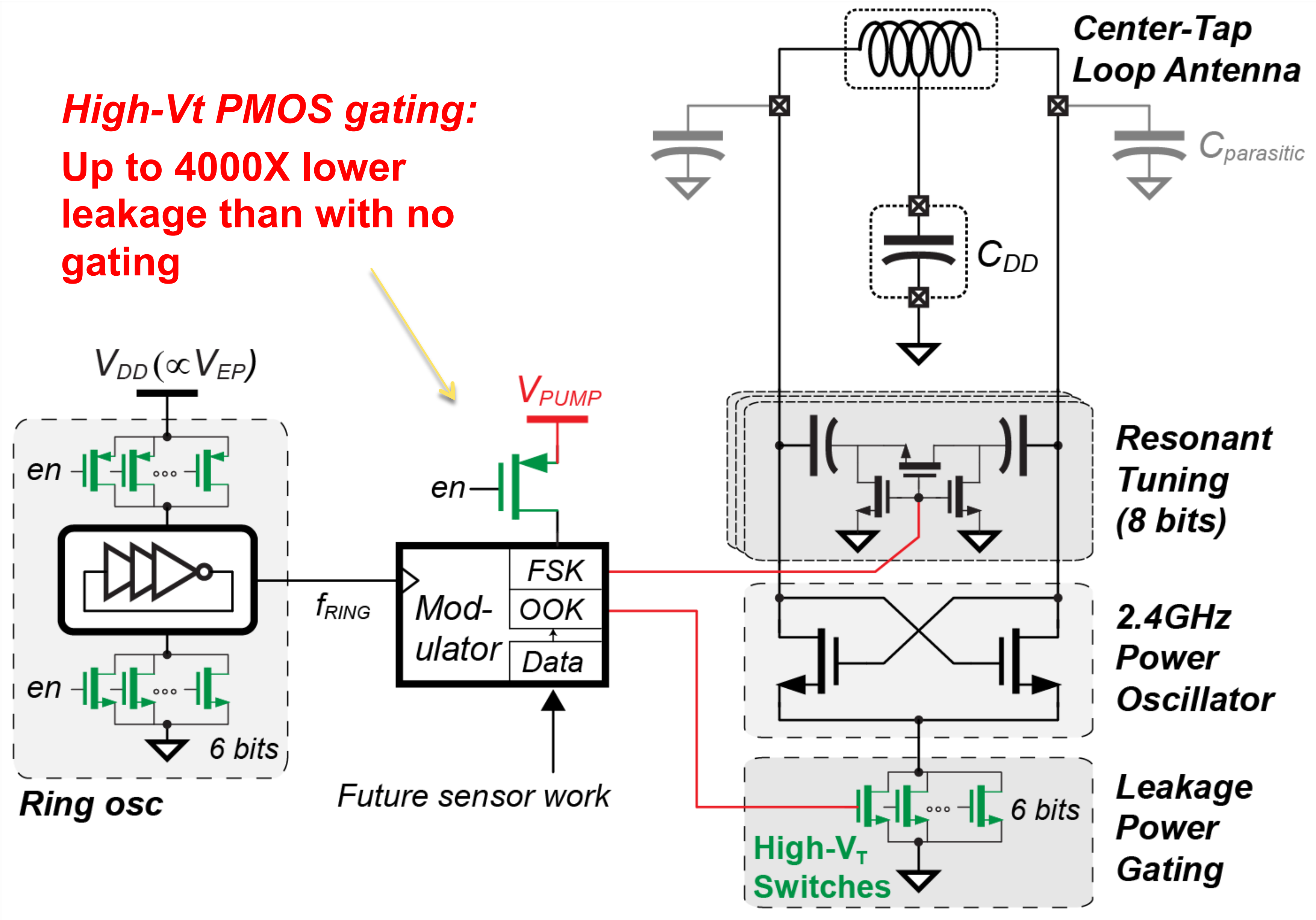
Leakage Power
from Output: <1pW

- **Use "old" digital tricks – "reverse biasing"**

Pico-Powered Transmitter!

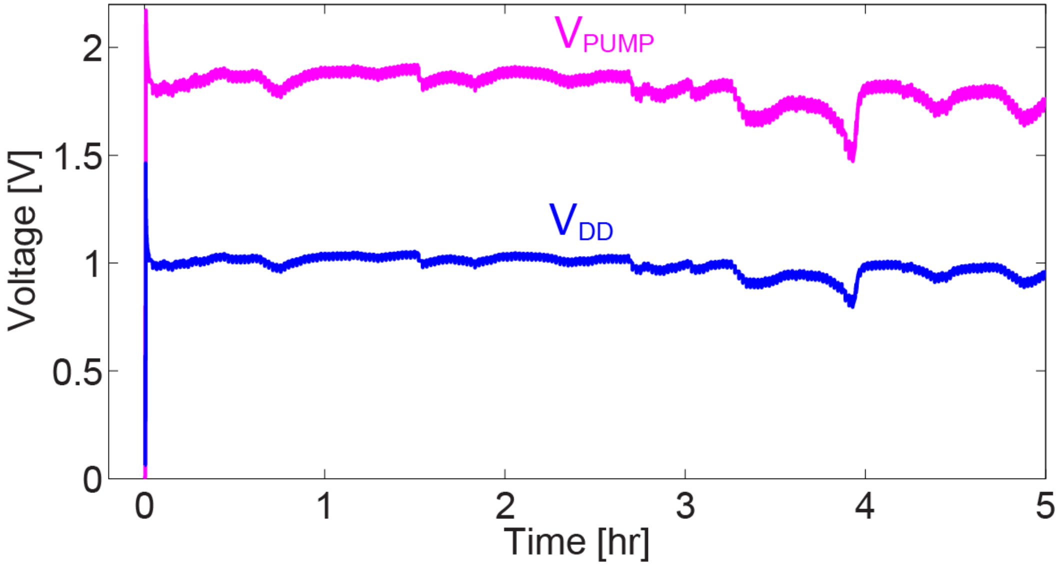
High-Vt PMOS gating:

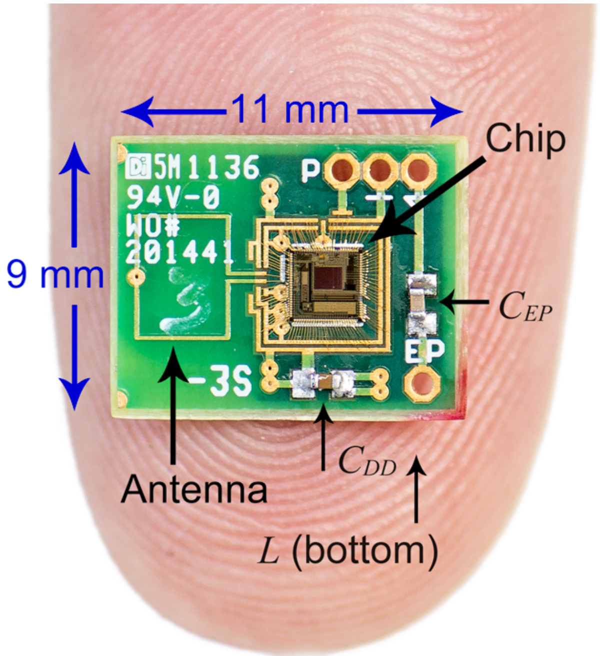
Up to 4000X lower leakage than with no gating

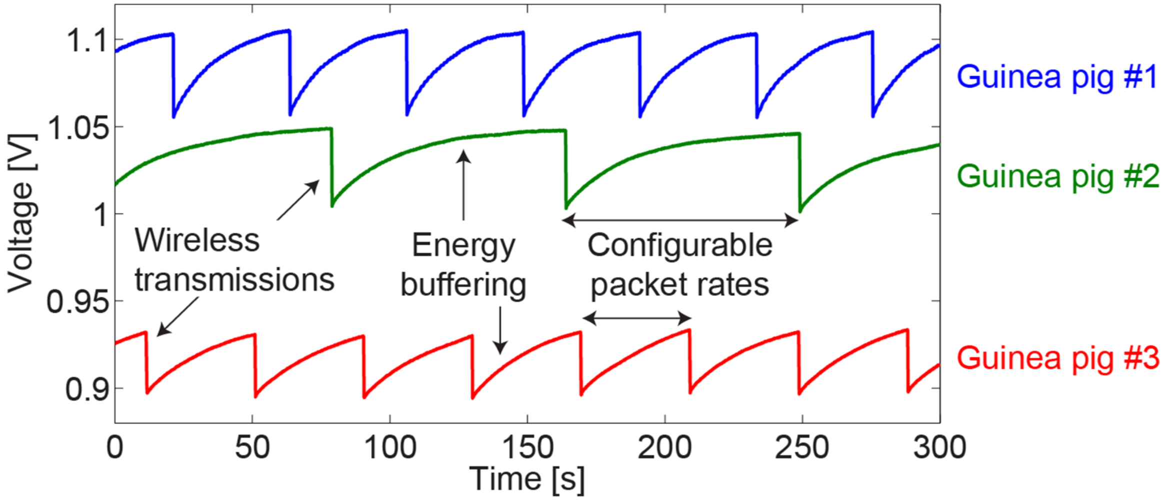


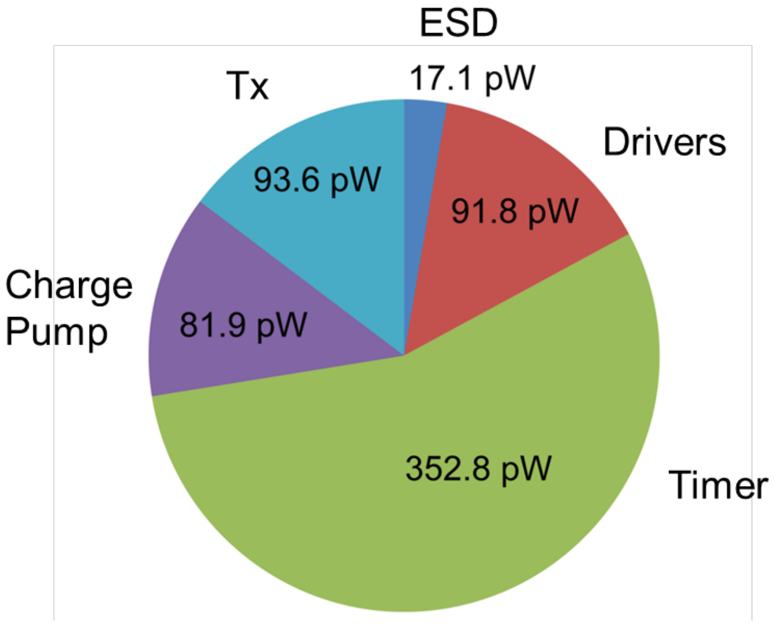
Fine Grained Power Gating

System Measurements





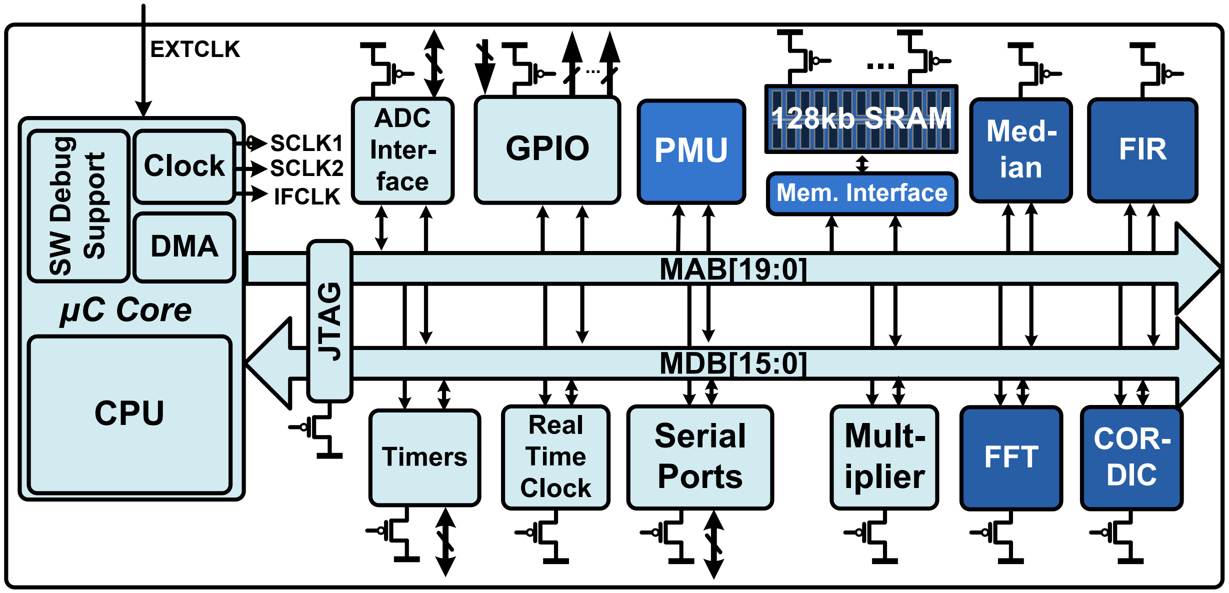


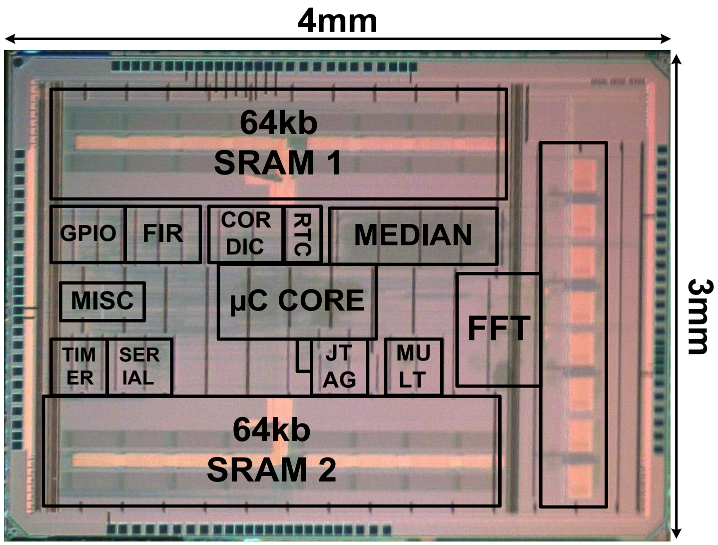


Directions in Ultra-low-Power Processing for IoT Systems

- Use of hardware accelerators
- Use of non-volatile processing for variable energy
- Ultra-low-voltage operations using parallelism
- Activity driven processing
- Light-weight machine learning for data reduction

Biomedical MSP-430 Processor with Hardware Accelerators



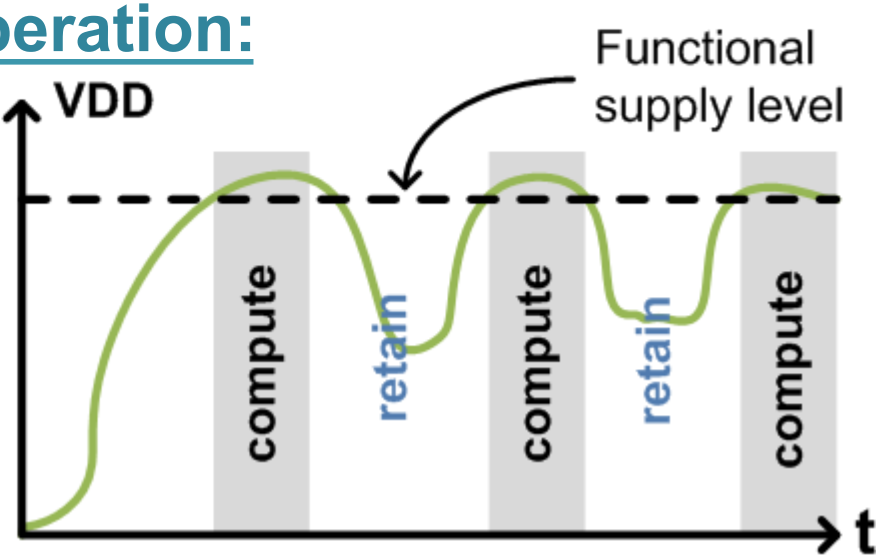


Joyce Kwong
[ESSCIRC ’10]

- 100-1000x reduction in energy by using accelerators
- Operation down to 0.5V – techniques can be combined
- Accelerators reduce overall energy by >10x in complete applications compared to CPU-only approach
  - EEG feature extraction for seizure detection: **10.2x savings**
  - EKG analysis: **11.5x savings**

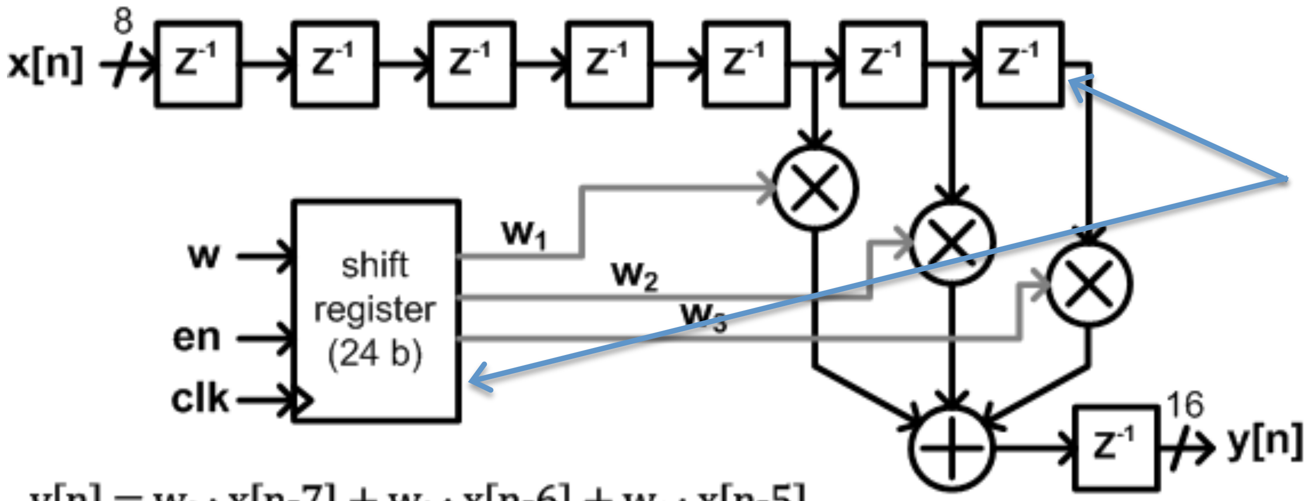
Non-Volatile Processor

Desired operation:



Replace all flip-flops with Non-volatile D Flip-Flop (NVDFF)

FIR filter test-case:

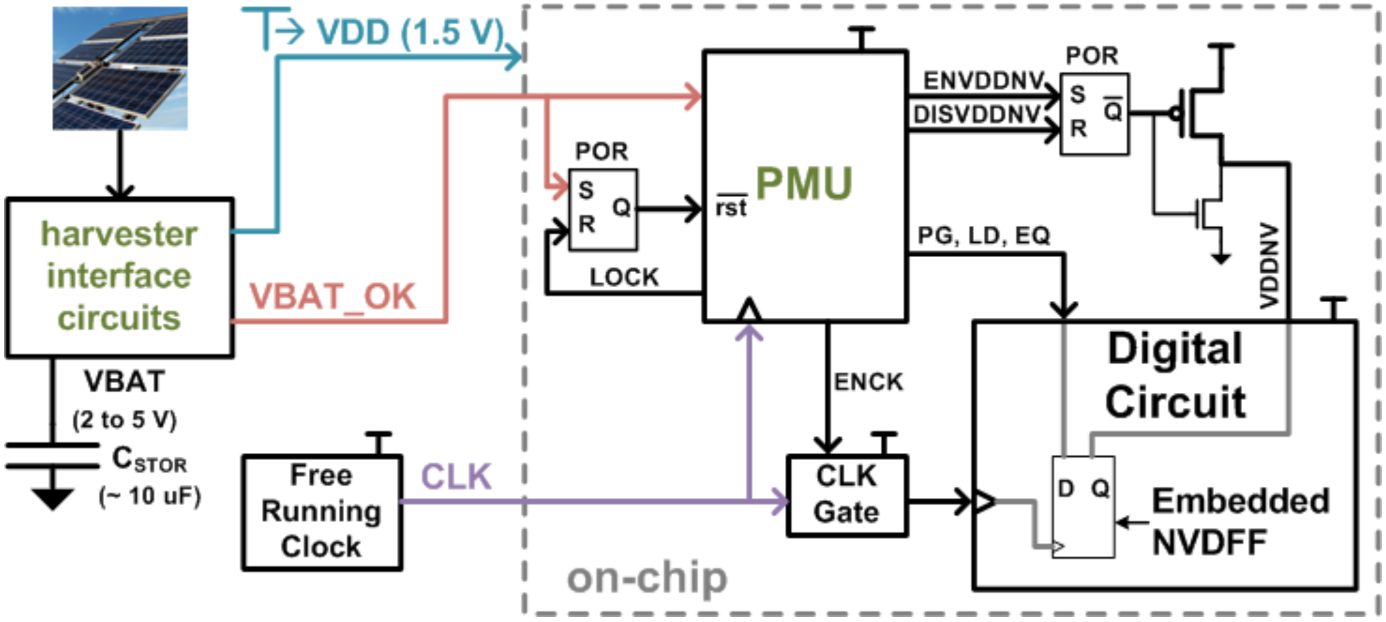


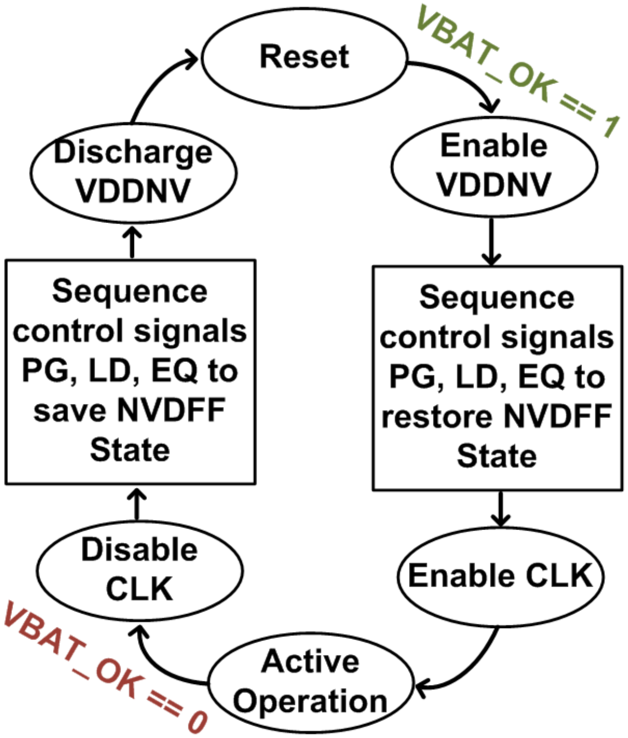
$$y[n] = w_3 \cdot x[n\text{-}7] + w_2 \cdot x[n\text{-}6] + w_1 \cdot x[n\text{-}5]$$

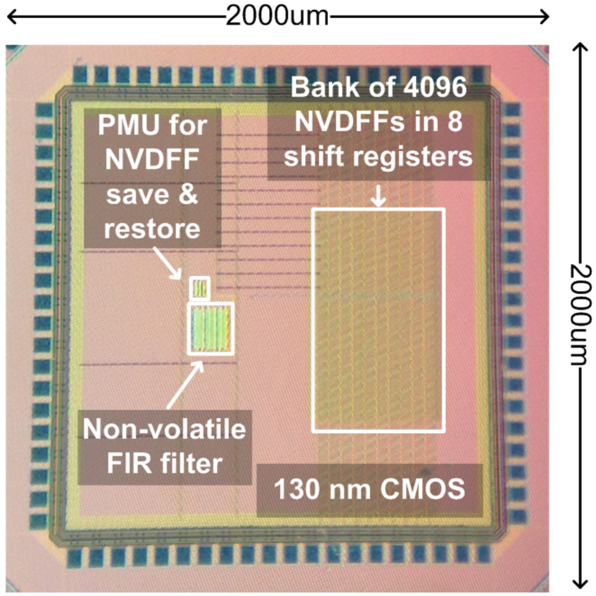
Embed non-volatile memory elements into registers

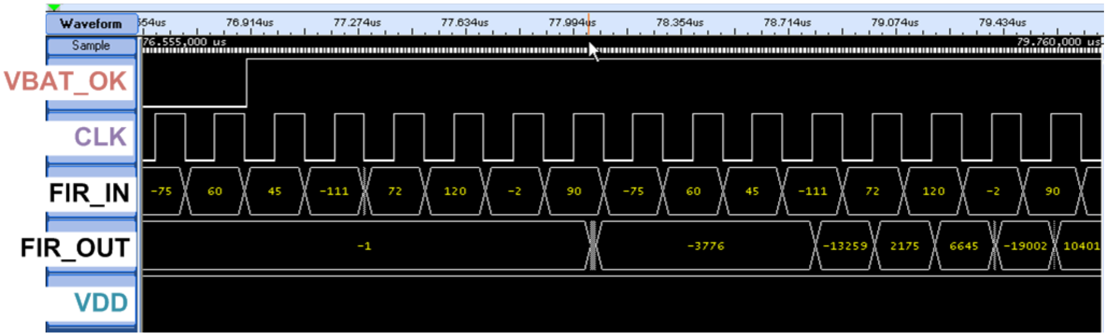
[M. Qazi, ISSCC 2013]

Computing Architecture with Energy Harvesting





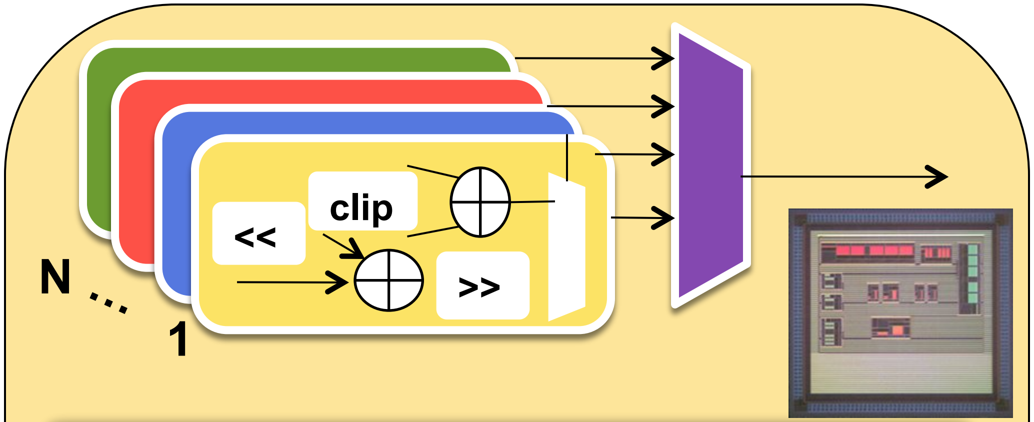




- **Rapid transition from sleep to active**

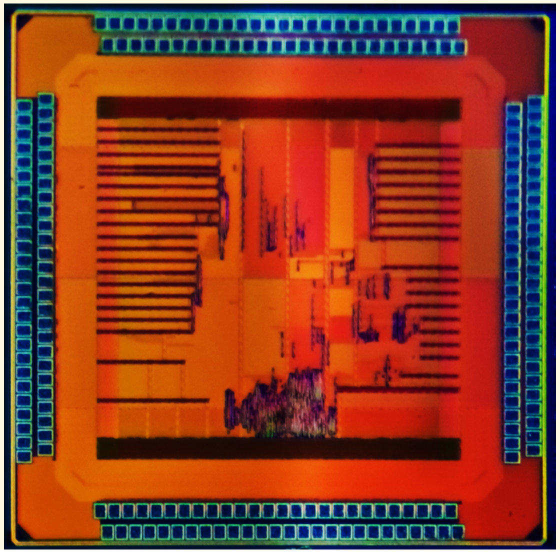
Ultra-Low-Power Using Parallelism

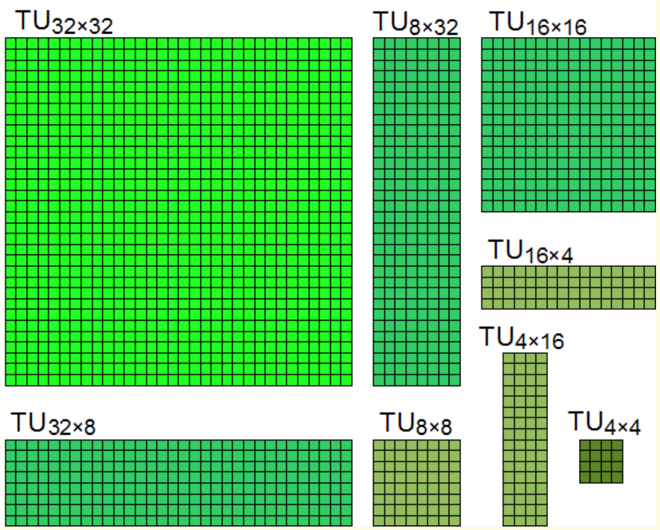
Parallel H.264



2mW H.264 decoder 720p in 65nm
(14x lower power)

Parallel H.265 (HEVC)





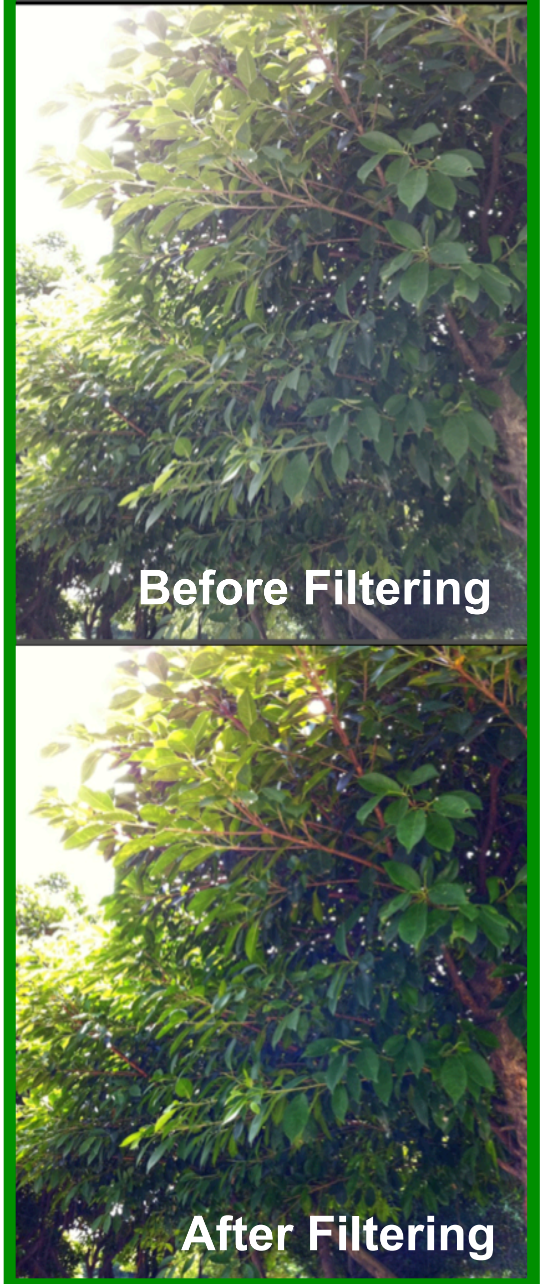
[C. Huang, ISSCC 2013]

Computational Photography

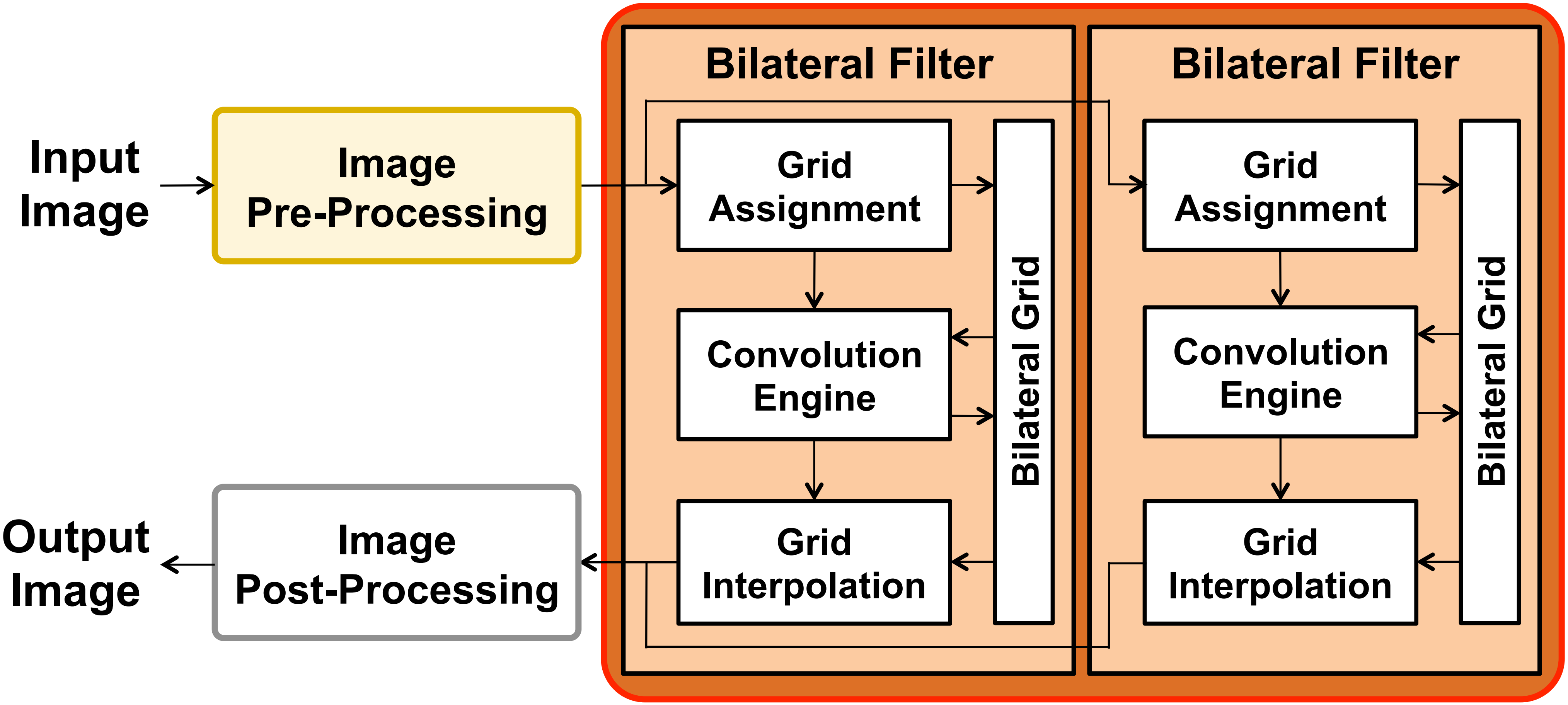
HDR Imaging

Low-light Enhancement

Glare Reduction

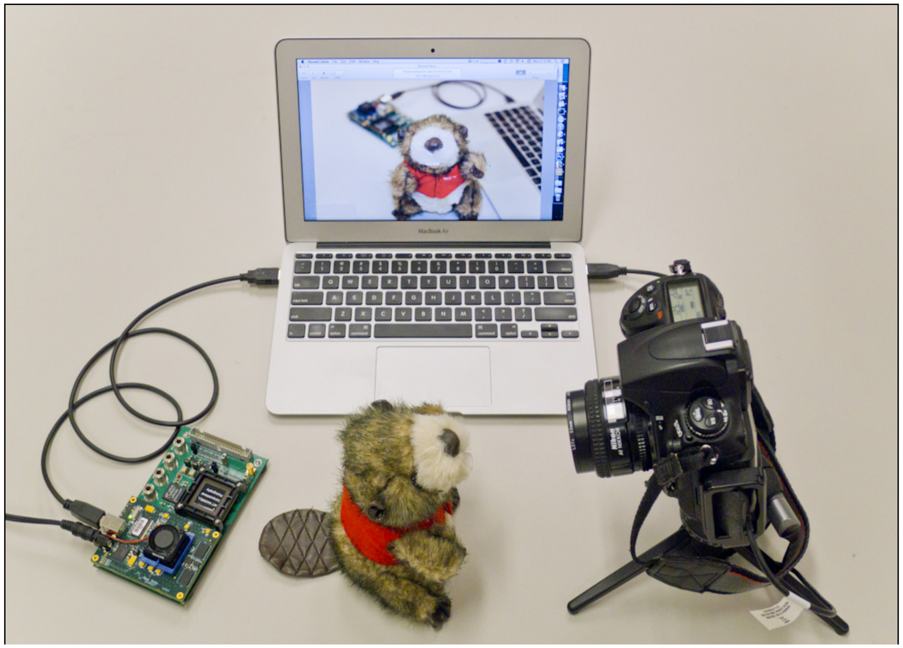


Application Specific Processor for Computational Photography



- Bilateral filtering using a 3D data structure called the Bilateral Grid
- Parallel processing for high throughput at low frequencies

Computational Photography

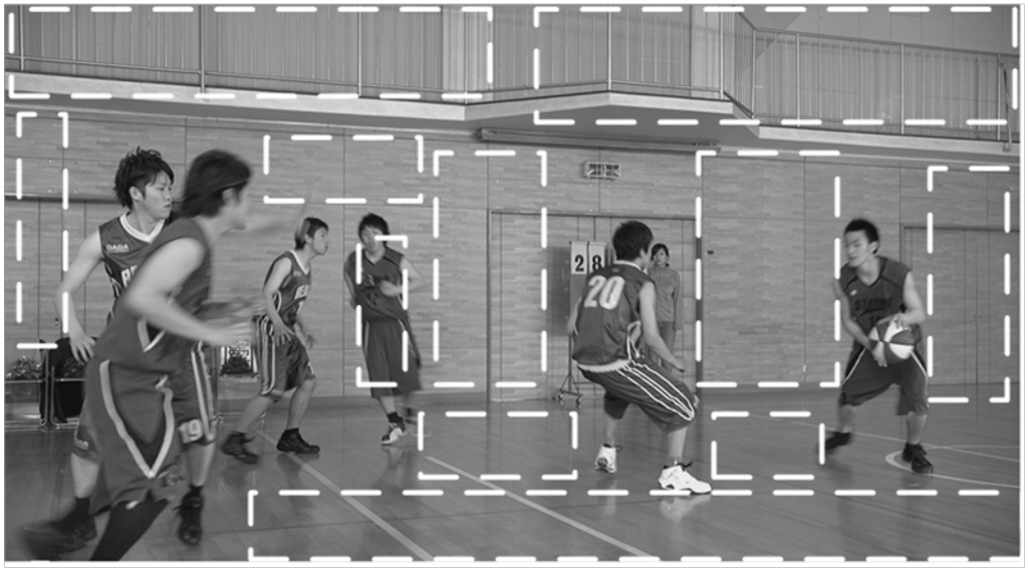


Processor	Technology (nm)	Frequency (MHz)	Power (mW)	Runtime* (s)	Energy* (mJ)
Intel Atom [24]	32	1800	870	4.96	4315
Qualcomm Snapdragon [25]	28	1500	760	5.19	3944
Samsung Exynos [26]	32	1700	1180	4.05	4779
TI OMAP [27]	45	1000	770	6.47	4981
This Work	40	98	17.8	0.771	13.7

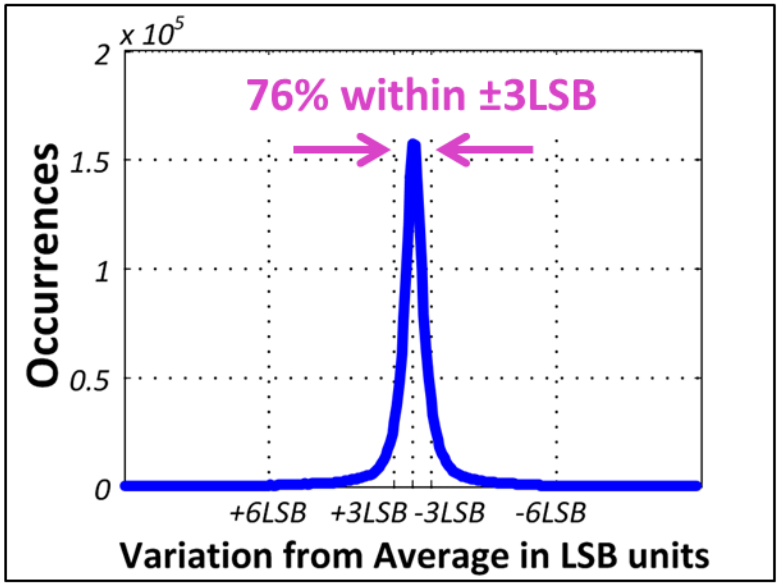
Rithe, R., P. Raina, N. Ickes, S. V. Tenneti, A. P. Chandrakasan, "Reconfigurable Processor for Energy-Efficient Computational Photography," IEEE Journal of Solid-State Circuits, vol. 48, no. 11, pp. 2908-2919, Nov. 2013.

Exploiting Signal Statistics

1. **Correlation of Pixel Data**



Variation from a 16x16 Block average



2. **# of Read Accesses > # of Write Accesses**

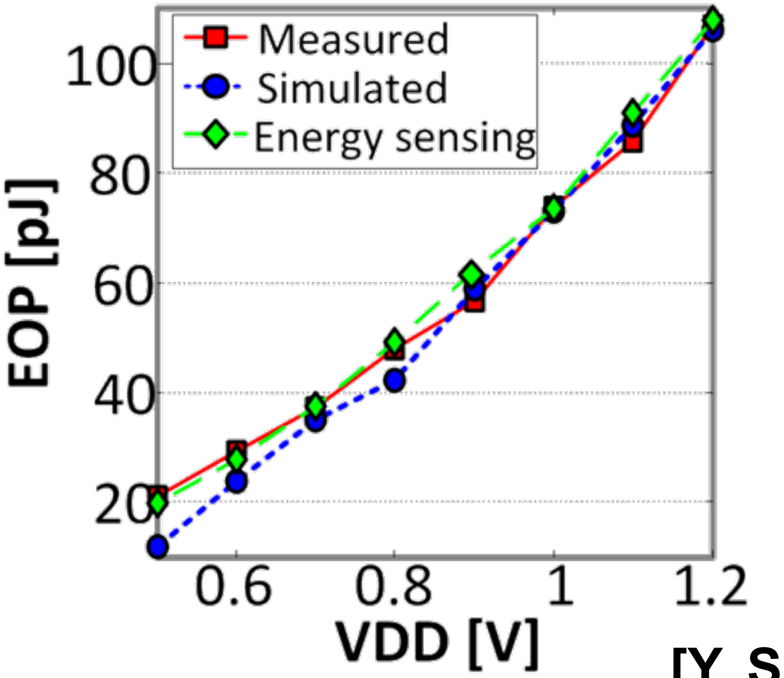
- Write once and read multiple times
  - Data reuse between consecutive blocks

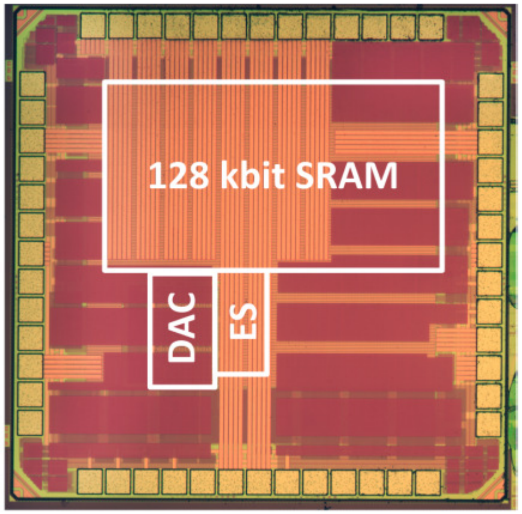
Reduce energy/access in read accesses by utilizing correlation of pixel data

[Mahmut Sinangil, ISSCC 2013]

Digital Energy Metering

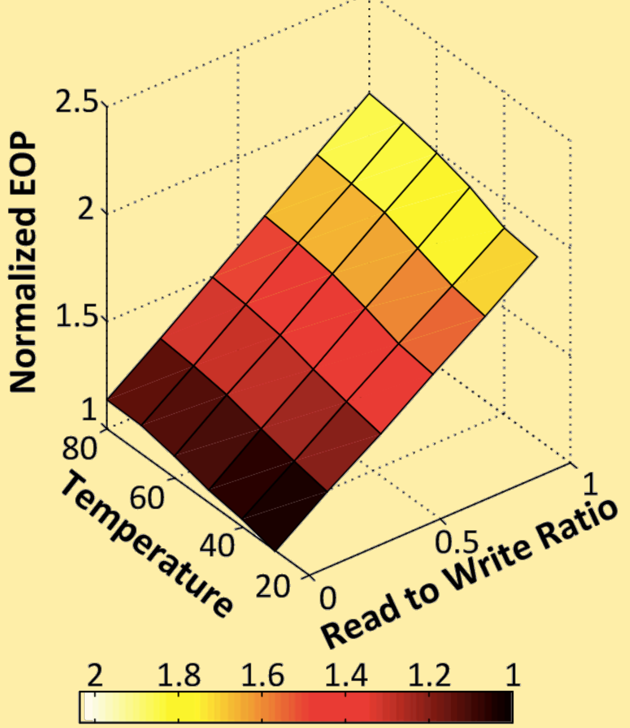
- **Energy Monitoring Circuit Operation:**
  - **An off-chip storage capacitor (C_{sto}) is used to power up the circuit during energy monitoring**
  - **If the voltage over C_{sto} drops by ΔV from V_1 to V_2 in N cycles, energy per operation (EOP) can be approximated as:** $C_{sto} \times V_1 \times \Delta V / N$





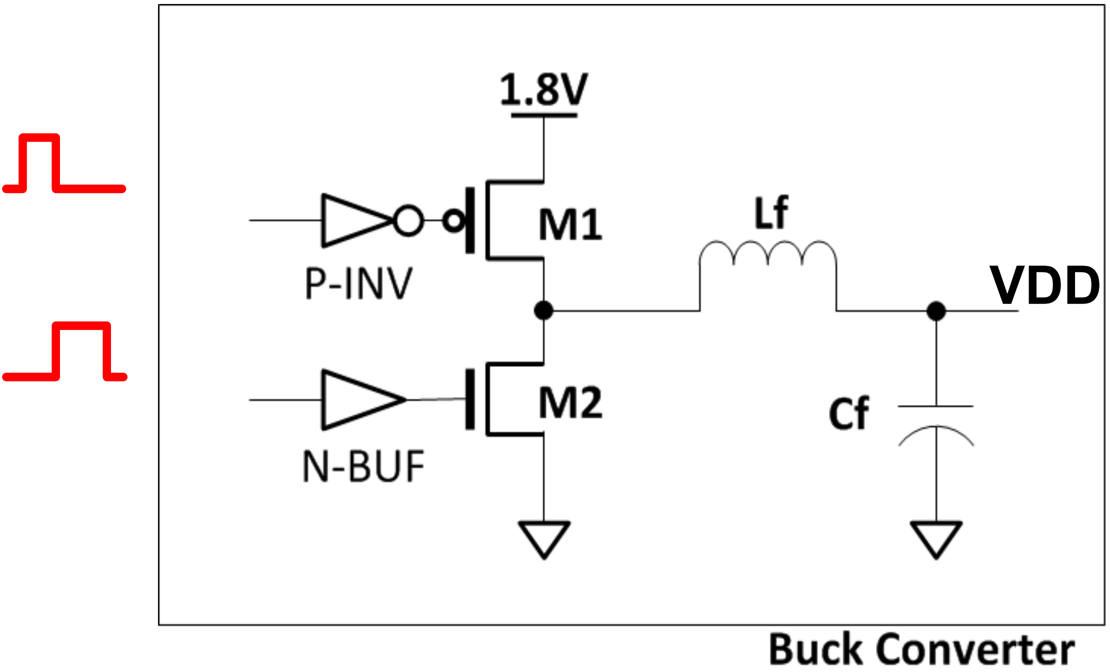
[Y. Sinangil, A-SSCC '12]

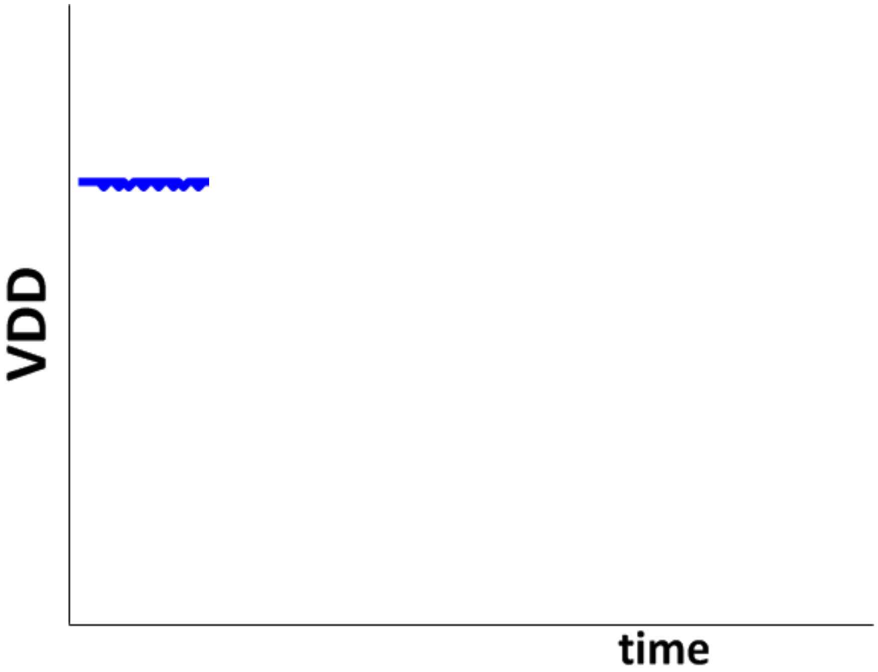
Measured Energy per Operation at VDD=800mV, f=1MHz



•measurement result:
2x change in energy per operation is observed due to transient effects

Energy Monitoring Circuit (1/3)

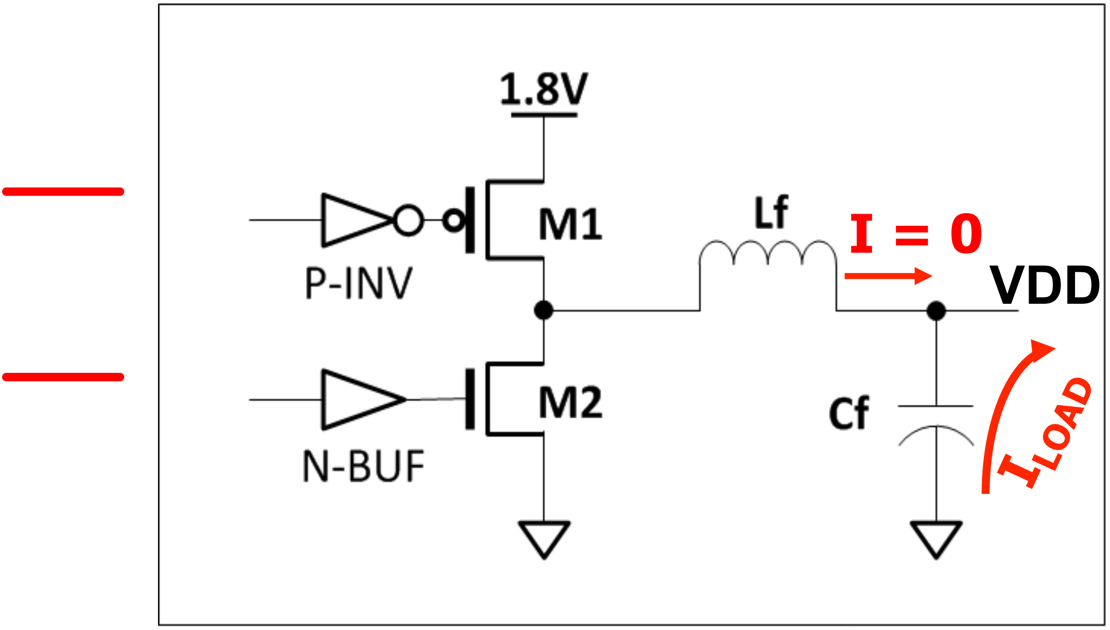




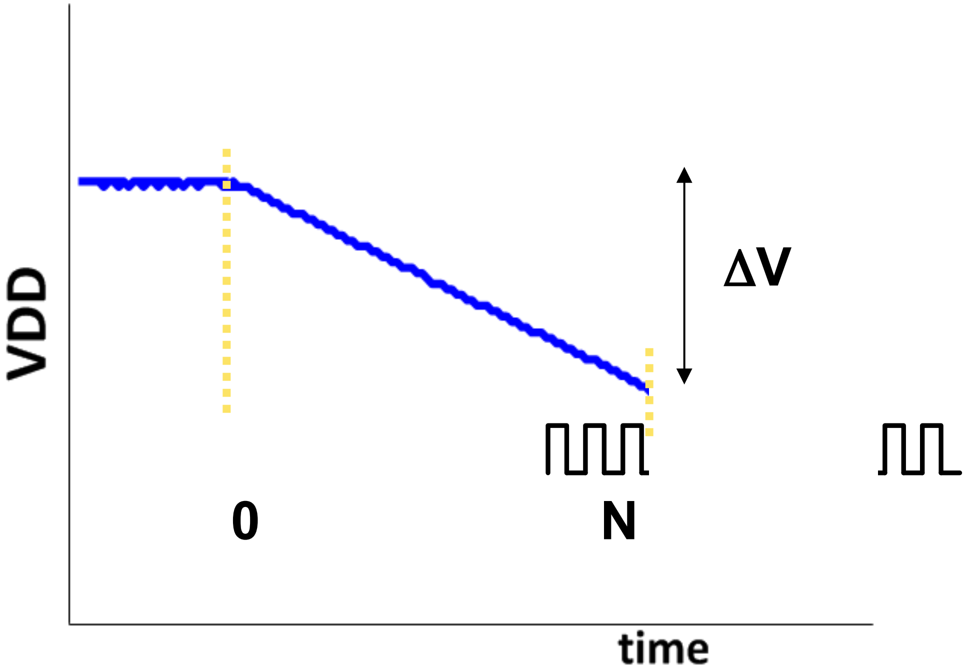
- **implemented and demonstrated with integrated power management circuits**

STEP 1 – Normal Operation: Buck Converter powers up the system

Energy Monitoring Circuit (2/3)

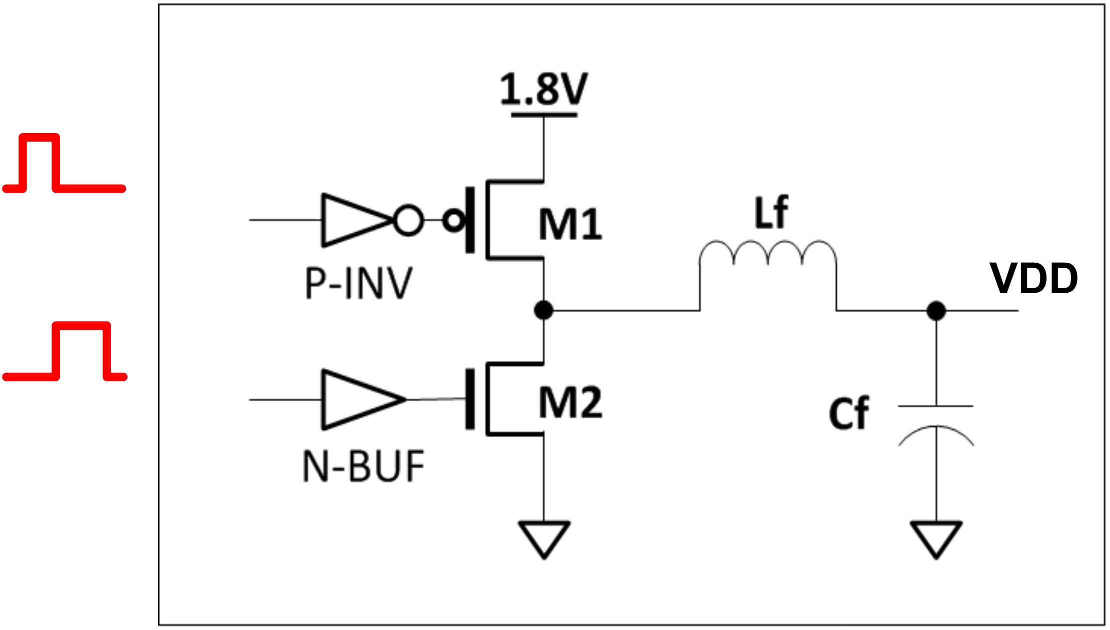


Buck Converter

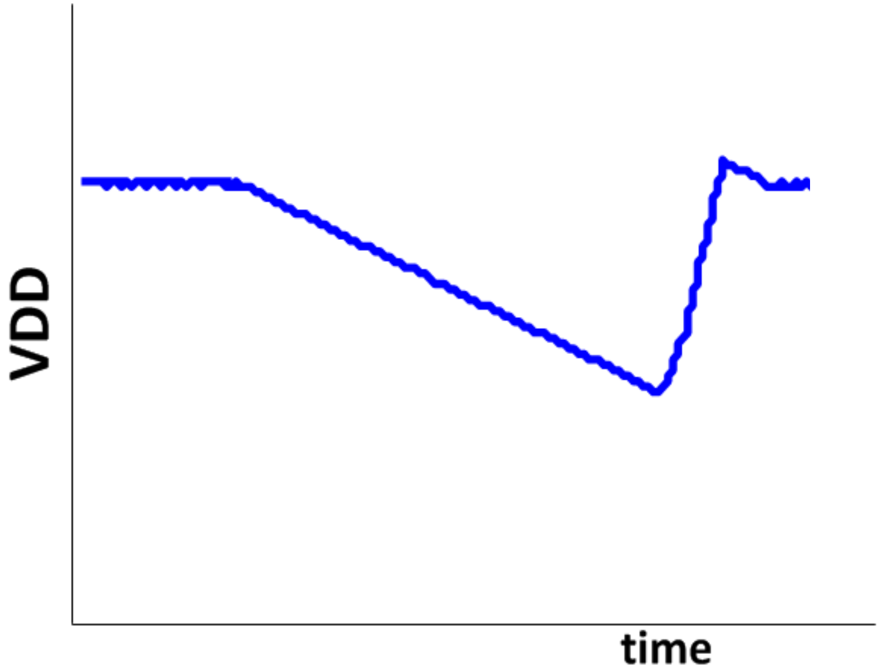


STEP 2 - Discharge: Cf is discharged from V1 to (V1 – ΔV) by I_{LOAD} in N cycles

Energy Monitoring Circuit (3/3)



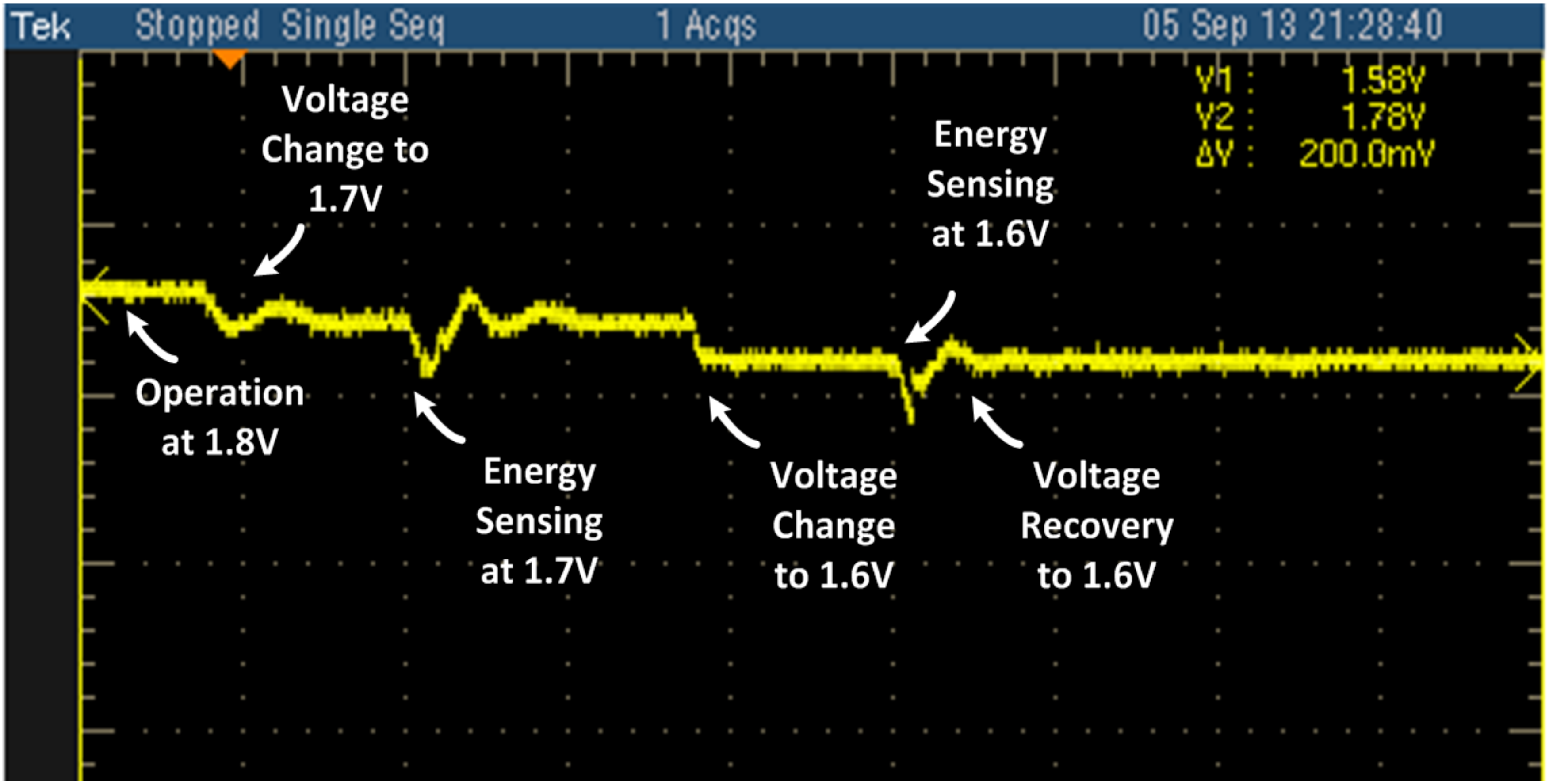
Buck Converter



STEP 3 – Recovery: Voltage is restored to initial VDD.

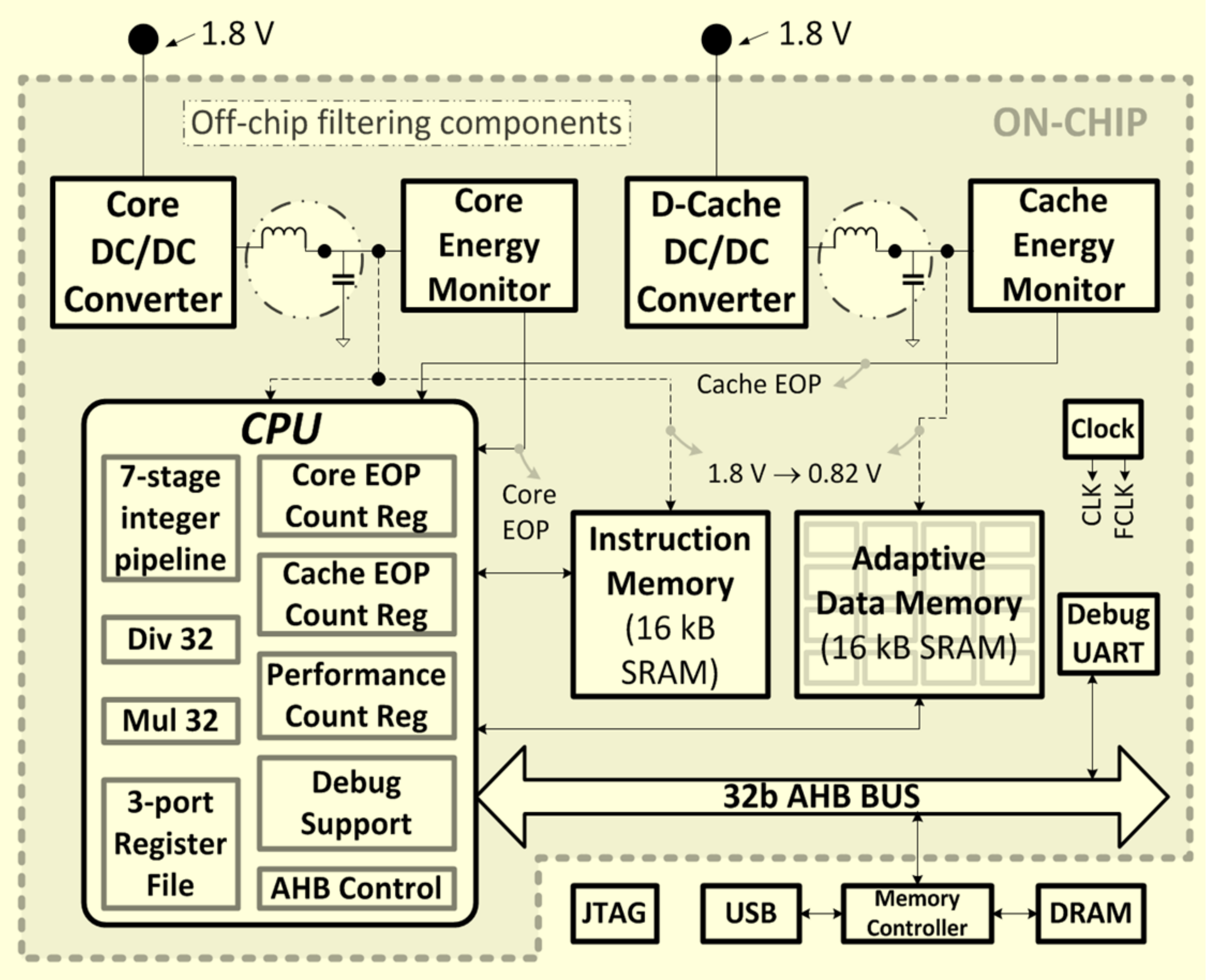
Energy per operation is measured as CF x V1 x ΔV / N

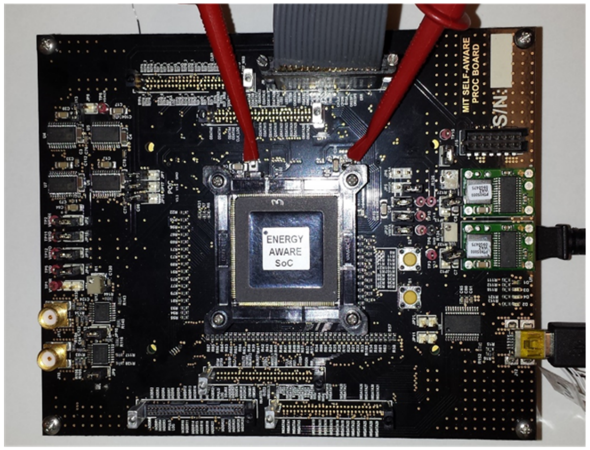
Sensor with Power Management Demonstrated



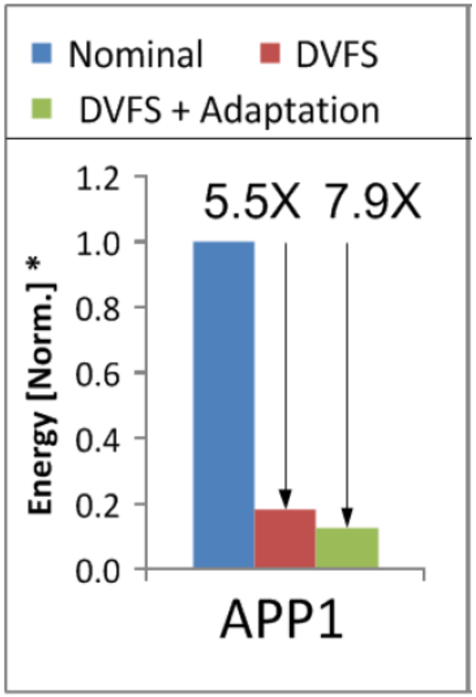
The operation of the system when performing energy monitoring and voltage changes

Self-Aware Test chip





TOP VIEW

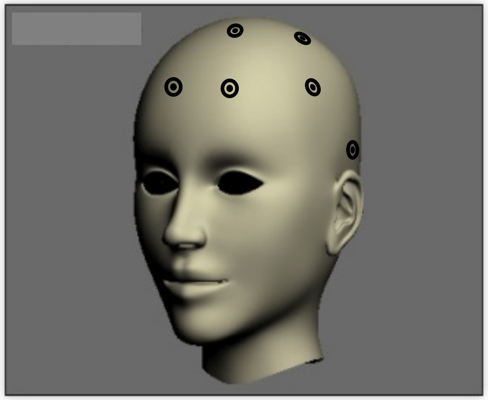


32x32

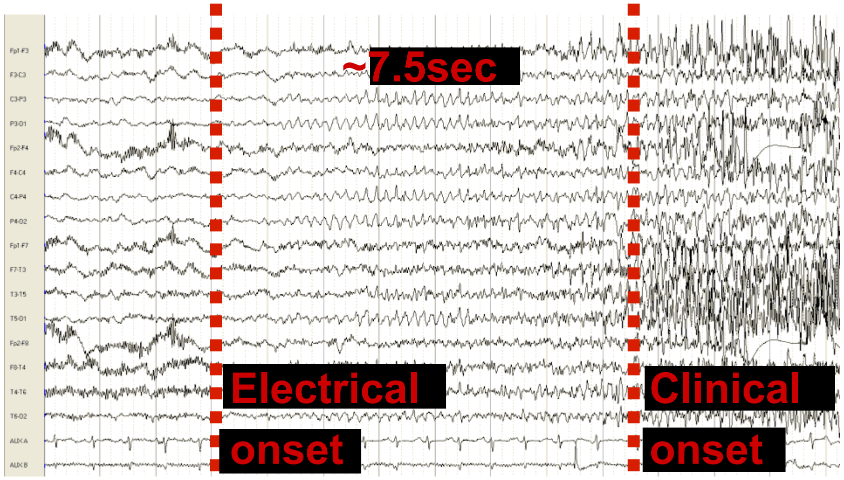
Matrix Transpose

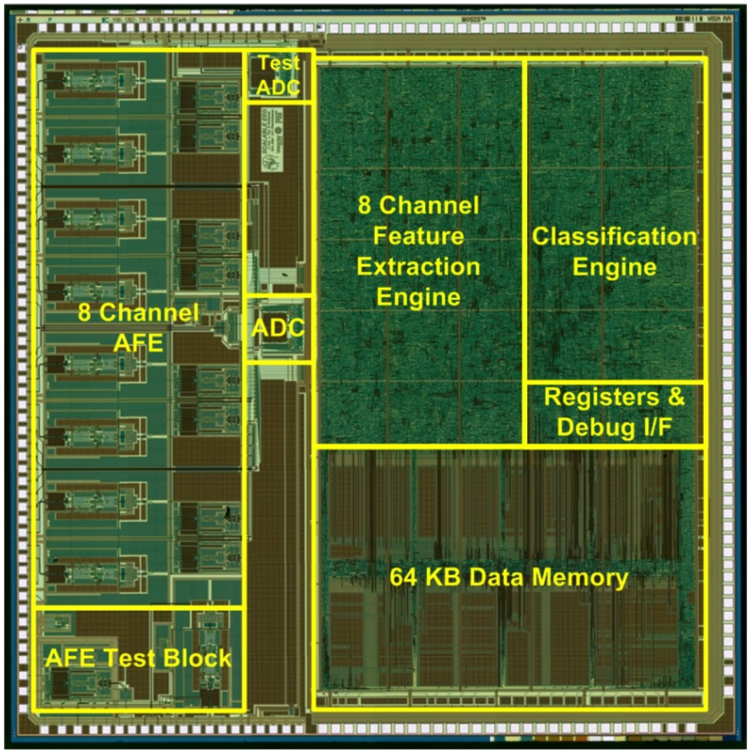
Y. Sinangil, S. M. Neuman, M. E. Sinangil, N. Ickes, G. Bezerra, E. Lau, J. E. Miller, H. C. Hoffmann, S. Devadas, and A. P. Chandrakasan, "A Self-Aware Processor SoC using Energy Monitors Integrated into Power Converters for Self-Adaptation," in Proc. Symposium on VLSI Circuits (VLSI), 2014.

Light-weight Machine Learning in Hardware



On-scalp Field Potentials (EEG):





Process	TSMC 0.18 μm 1P6M CMOS
Area	5.0 x 5.0 mm
Supply Voltage	1.8V (AFE) 1.0V (DBE, ADC)
Channel	1 to 8 Scalable
Input Dyn. Range	30-59 dB (4 step)
AFE Power	66μW
Bandwidth	30Hz / 100Hz
ADC	Fully Differential SAR ADC
	10b, 4-32KS/s
Classifier Type	Support Vector Machine
Latency	< 2s
Accuracy	84.4%
Efficiency	2.03μJ /Classification

Epileptic Seizure Onset Detection

[Jerald Yoo, ISSCC 2012]

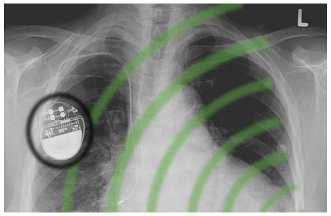
Security for IoT

IoT introduces many unique security challenges:

- ➢ Widely deployed sensors collecting private and sensitive data
- ➢ All interconnected and potentially accessible to attackers

Example attack scenarios:

- **Pacemakers can be hacked to cause unwanted stimulation**



- **Activity tracker logs can help an attacker profile users**

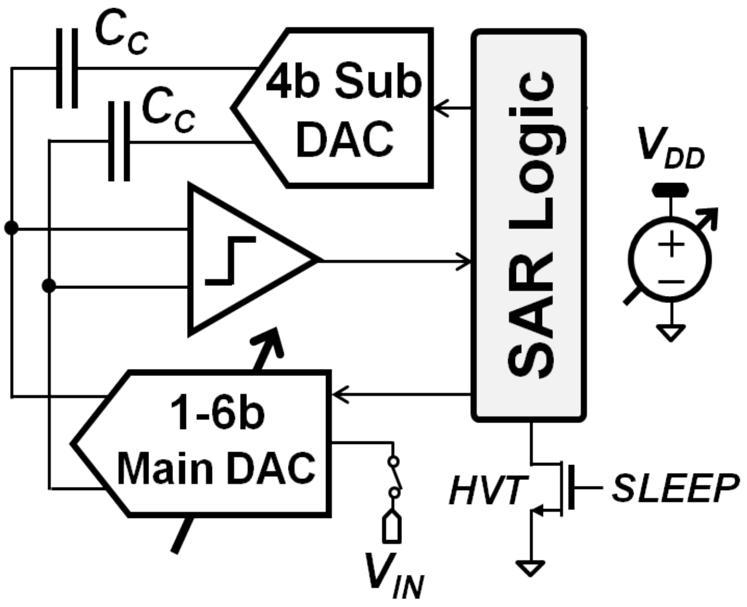
- **Home automation devices can be compromised to give attackers access**

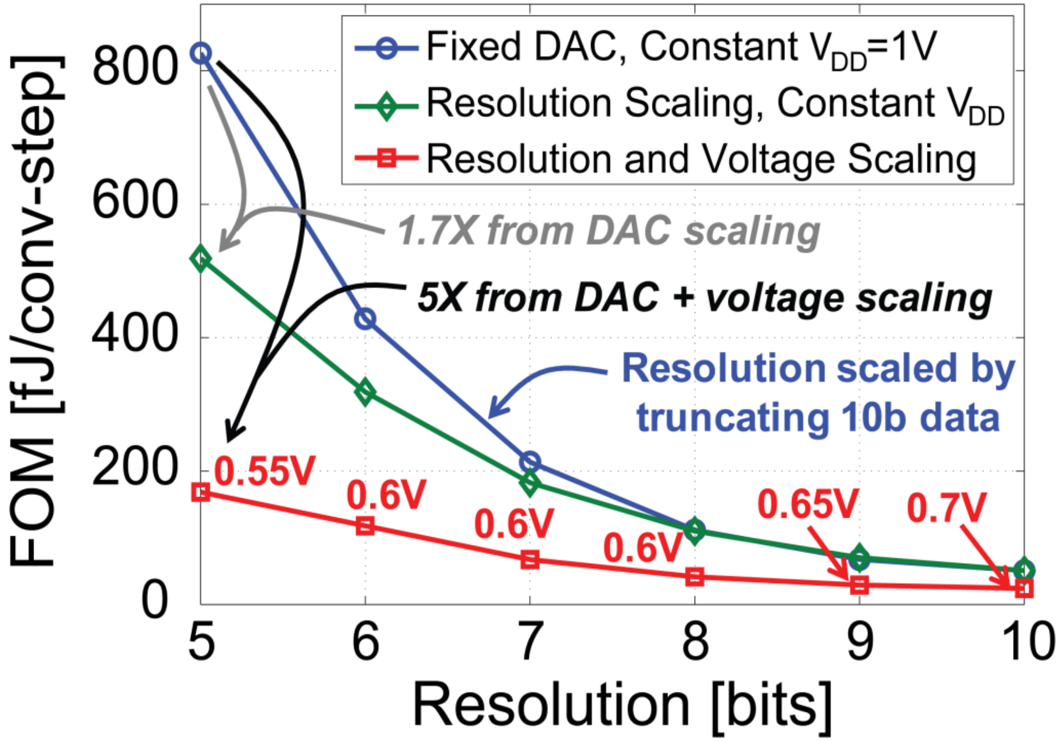
Opportunities

- **Implement new crypto primitives like FHE to enable secure systems**
- **System solutions to provide complete security for IoT applications**

A Voltage and Resolution Scalable SAR ADC

- Energy-efficient 5b to 10b resolution scalable DAC
- Voltage scalable from 0.4V (5kS/s) to 1V (2MS/s)
- Leakage power-gating important at low voltage/sample rates

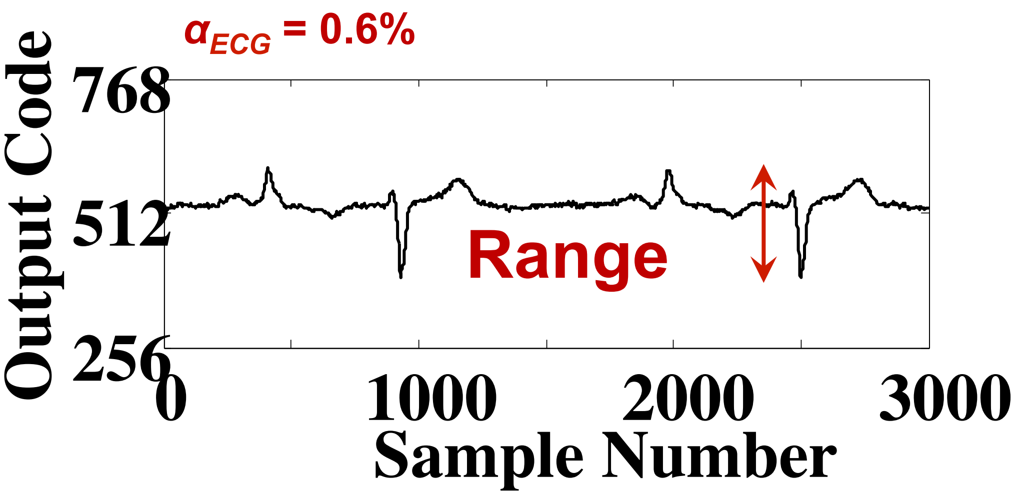




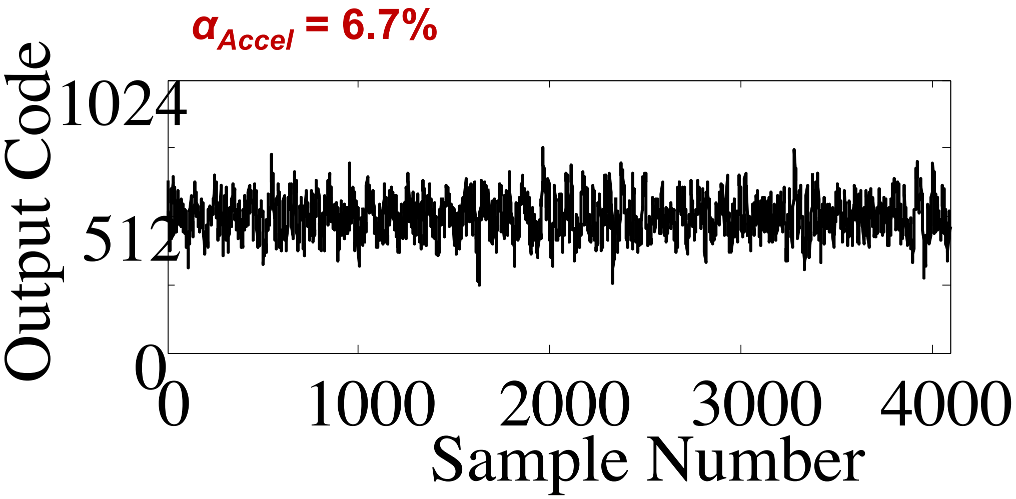
[M. Yip, ISSCC 2011]

Data Dependent SAR

$$\alpha = \langle code \rangle / range$$


$\alpha_{ECG} = 0.6\%$

ECG Signal, 1 kS/s

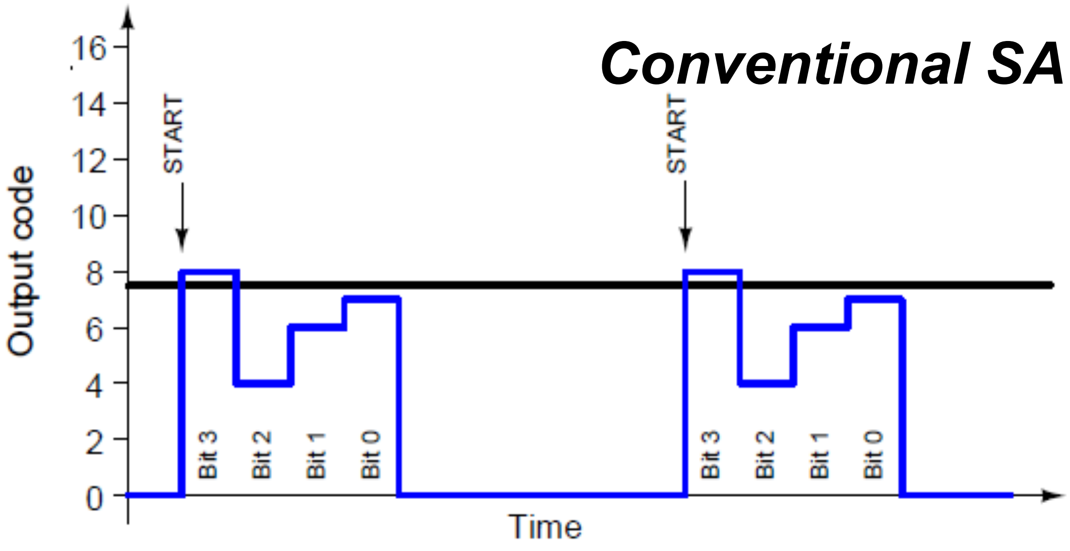

$\alpha_{Accel} = 6.7\%$

Vibration Signal, 5 kS/s

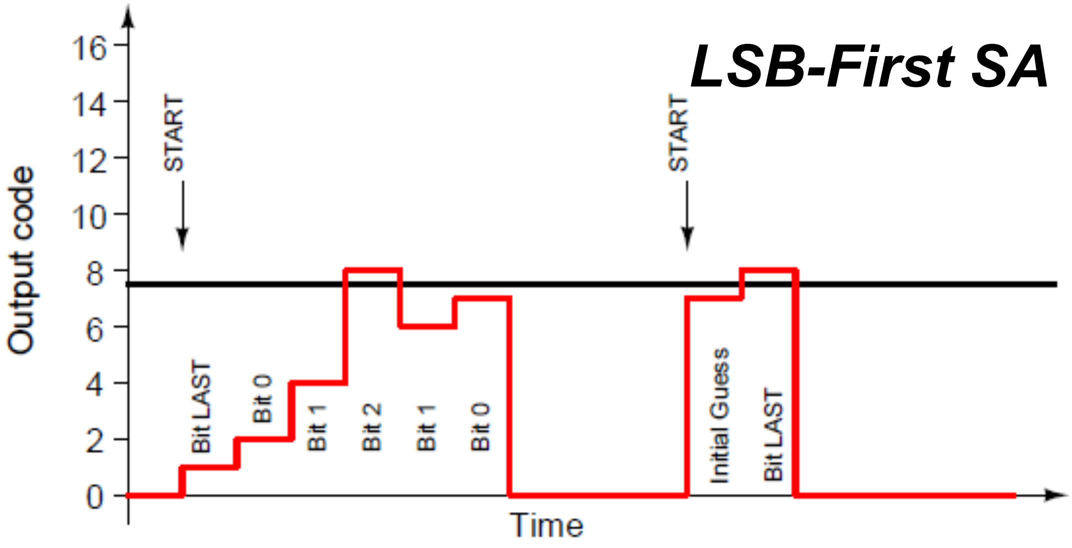
Data Dependent SAR

- Conventional SA always uses the same initial guess

- Alter the algorithm to exploit low signal activity
  - Start search at previous sample.
  - Use fewer bitcycles when initial guess is close to final output code.

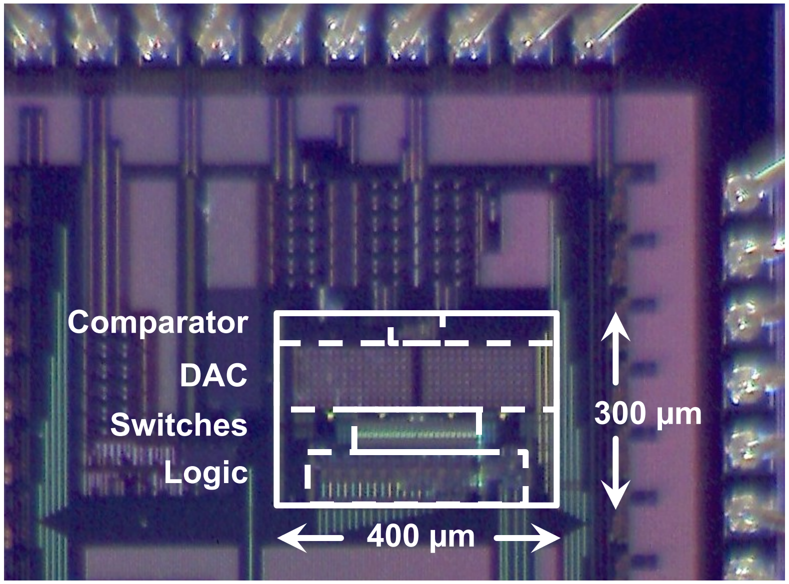


Conventional SA

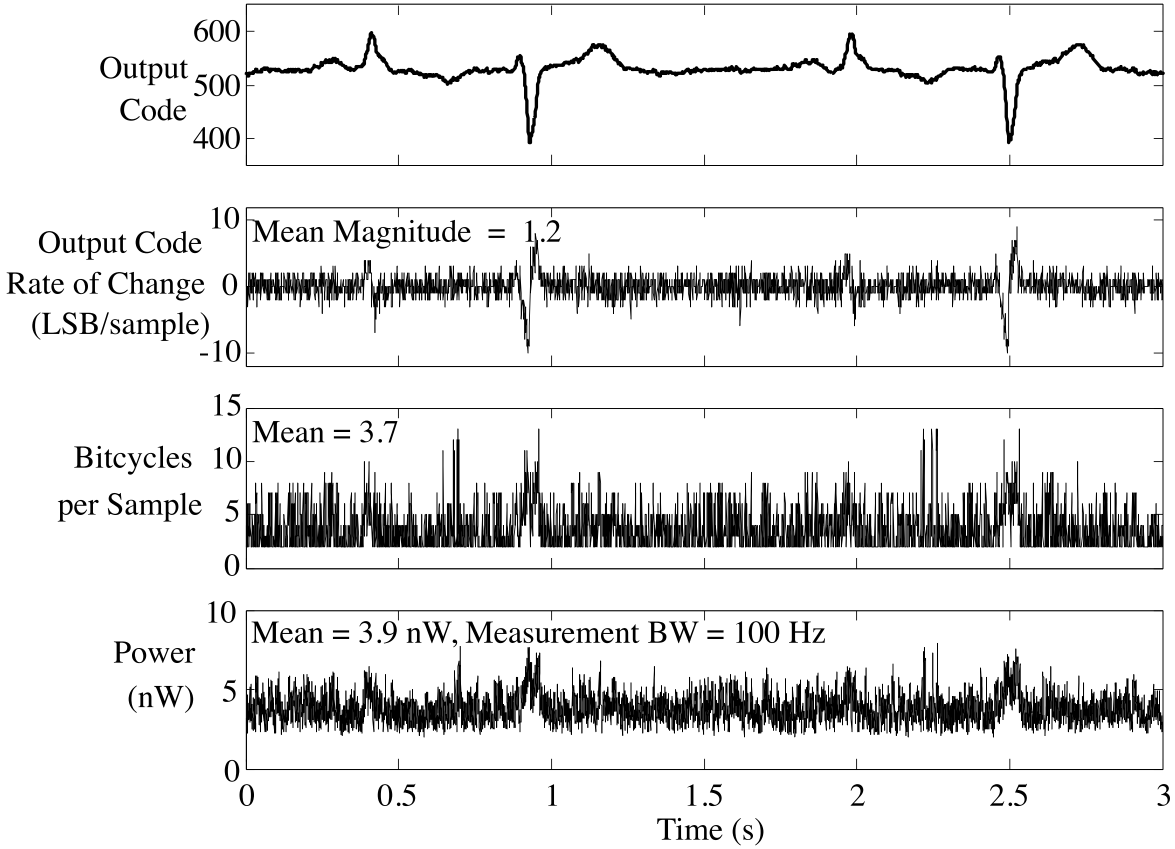


LSB-First SA

Measurement Results



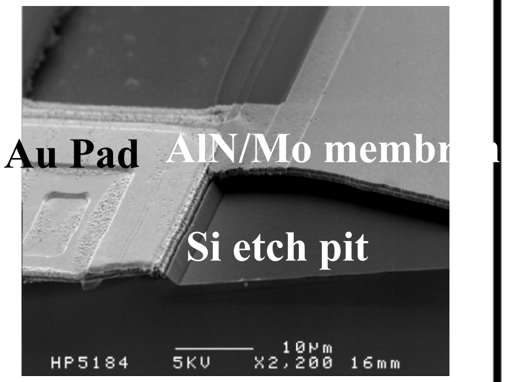
0.18µm General Purpose CMOS

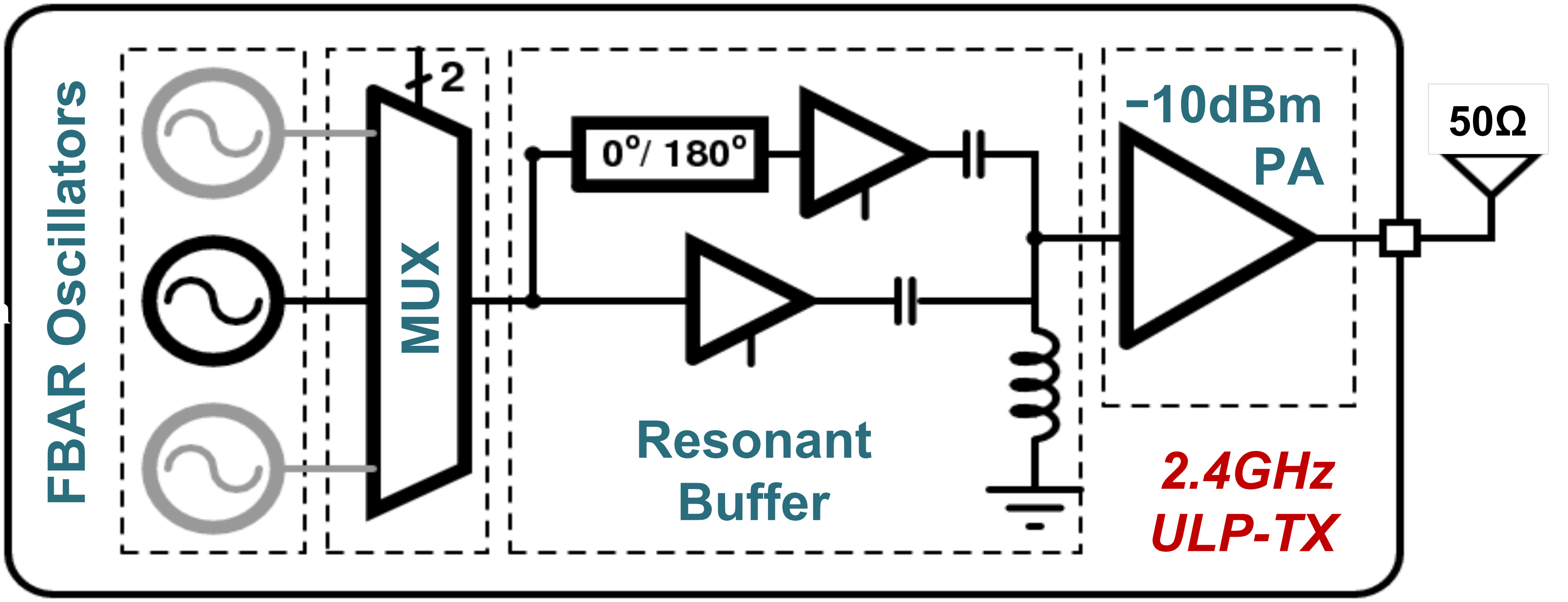


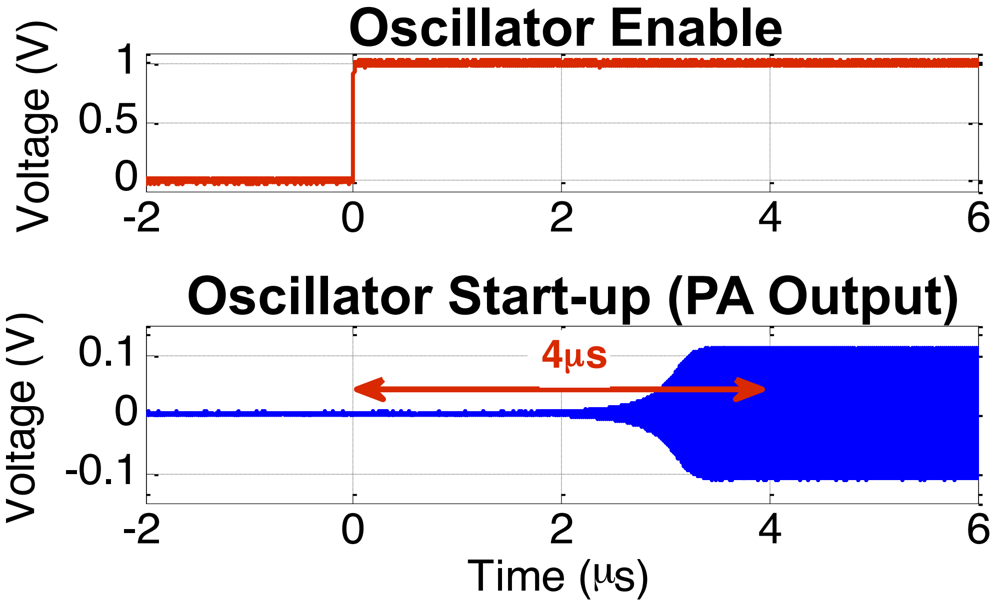
ADC response to ECG test input signal at VDD=0.5V and f_S=1 kHz

Yaul, F. M., A. P. Chandrakasan, "A 10b 0.6nW SAR ADC with Data-Dependent Energy Savings Using LSB-First Successive Approximation," IEEE International Solid State Circuits Conference (ISSCC), Feb 2014.

Multi-Channel FBAR Transmitter





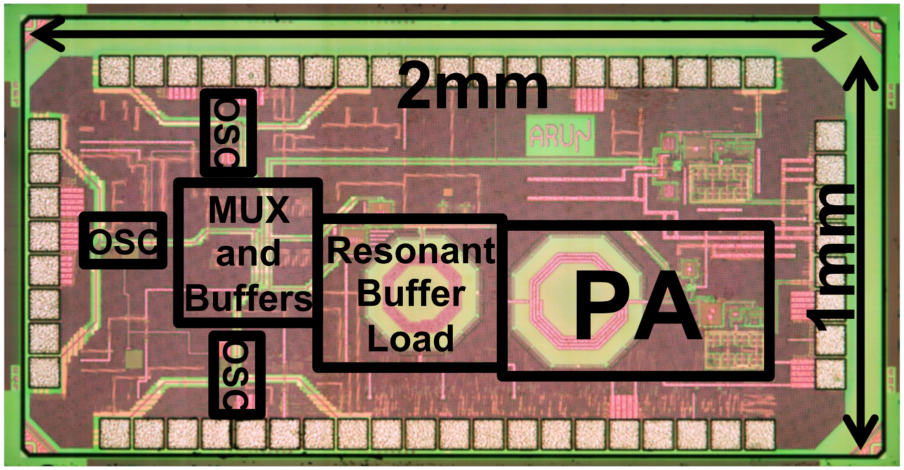


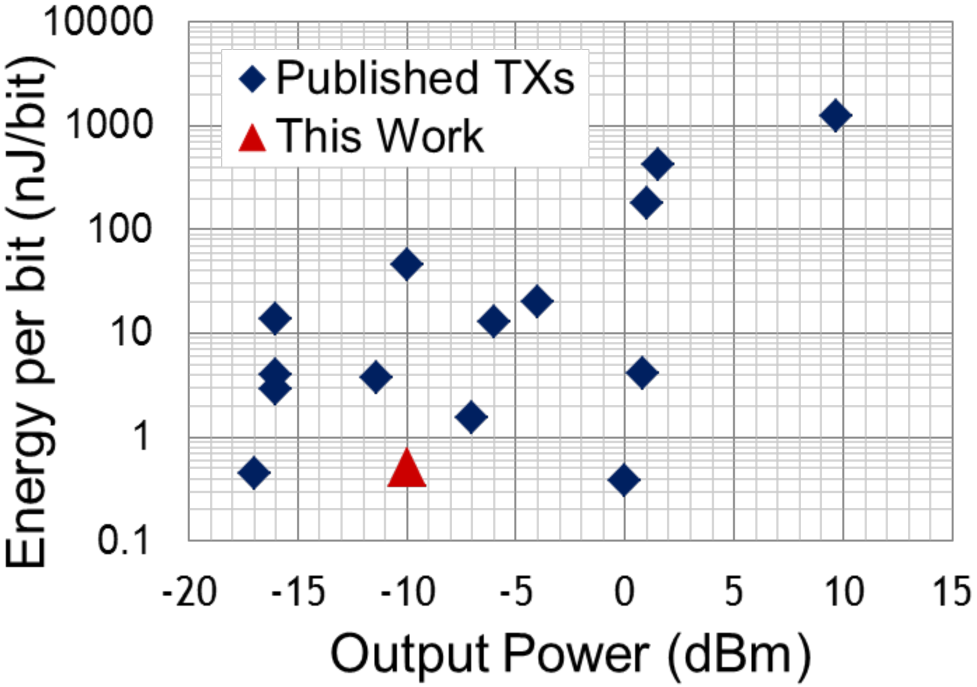
- Oscillator consumes 150µW from 0.7V supply
- Fast startup-time minimizes energy overhead

[A. Paidimarri, VLSI Symp. ‘12]

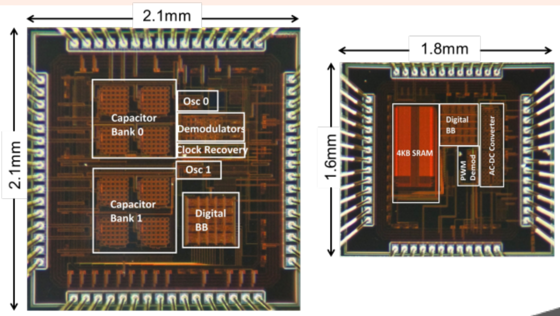
Transmitter Testchip

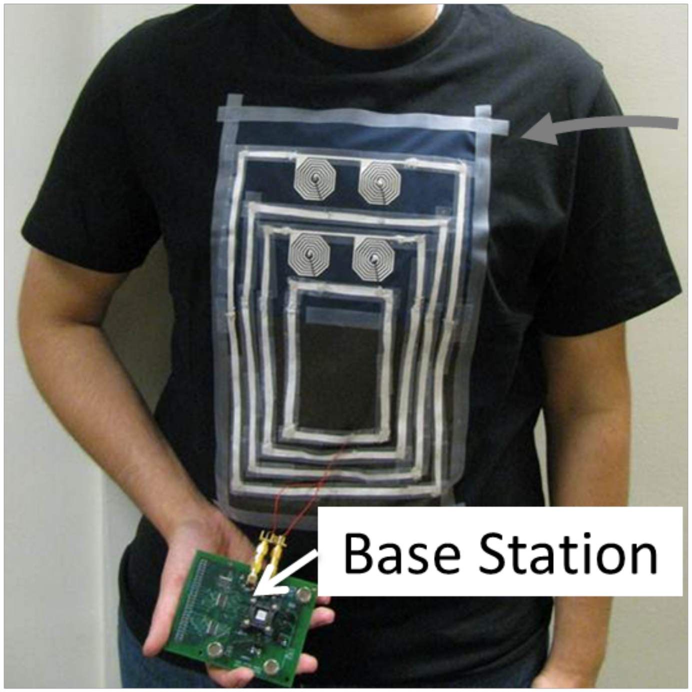
Technology	65nm CMOS
Supply	0.7V (RF), 1V (Switch)
Num. Chan.	3
Startup Time	4µs
Data Rate	1Mb/s
Phase Noise	−132dBc/Hz (at 1MHz)
P_{OUT}	−17.0dBm to −2.5dBm
Energy per bit and Average P_{OUT}	
OOK (Gauss) BPSK (SRRC) GMSK	440pJ/b at −12.5dBm 530pJ/b at −11.0dBm 550pJ/b at −10.0dBm



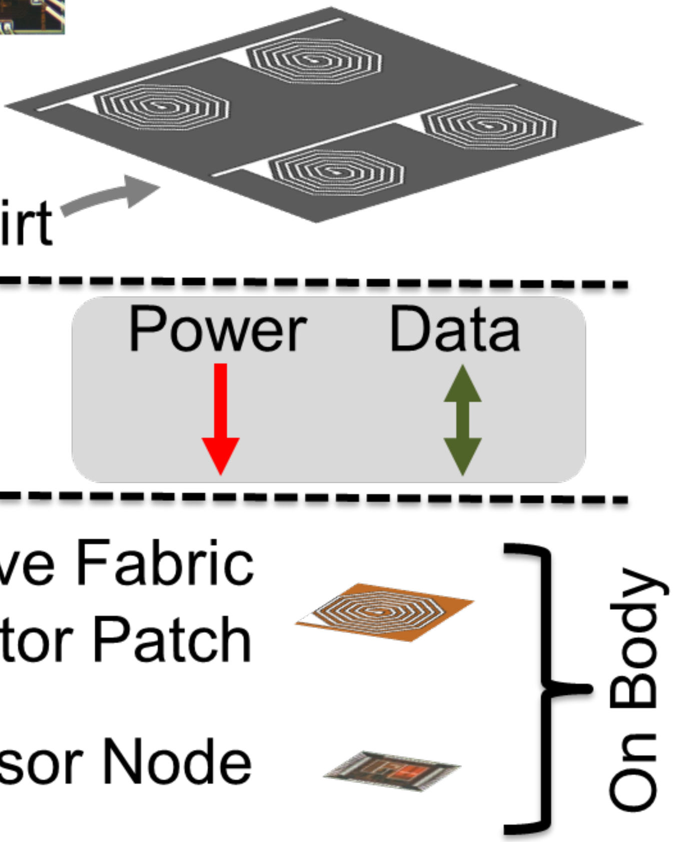


e-Textiles with Wireless Power/ Data Transfer





e-Textiles Shirt



Inductive Link

Power

Data

Adhesive Fabric Inductor Patch

Sensor Node

On Body

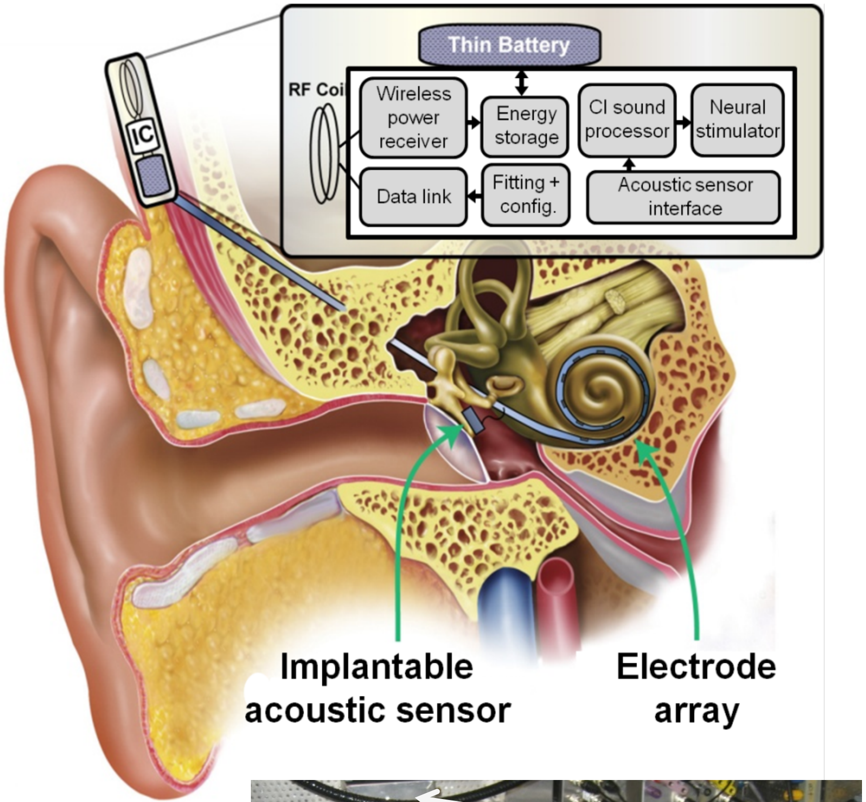
Network of diverse, remotely-powered sensors wirelessly linked to eTextiles

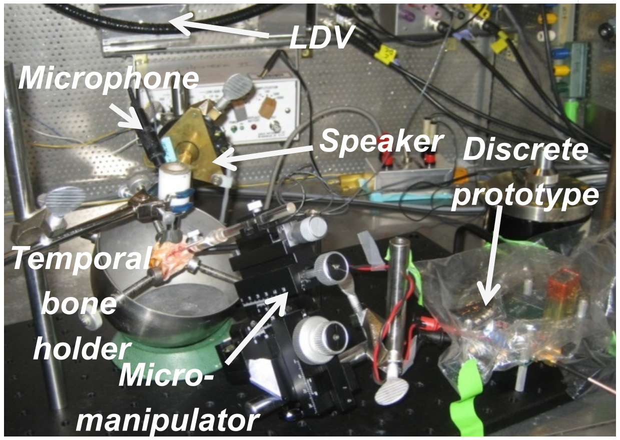
Nachiket Desai, ISSCC 2013

Putting it Together: Fully-Implantable Cochlear Implant

Conventional CI

Fully-Implantable Solution



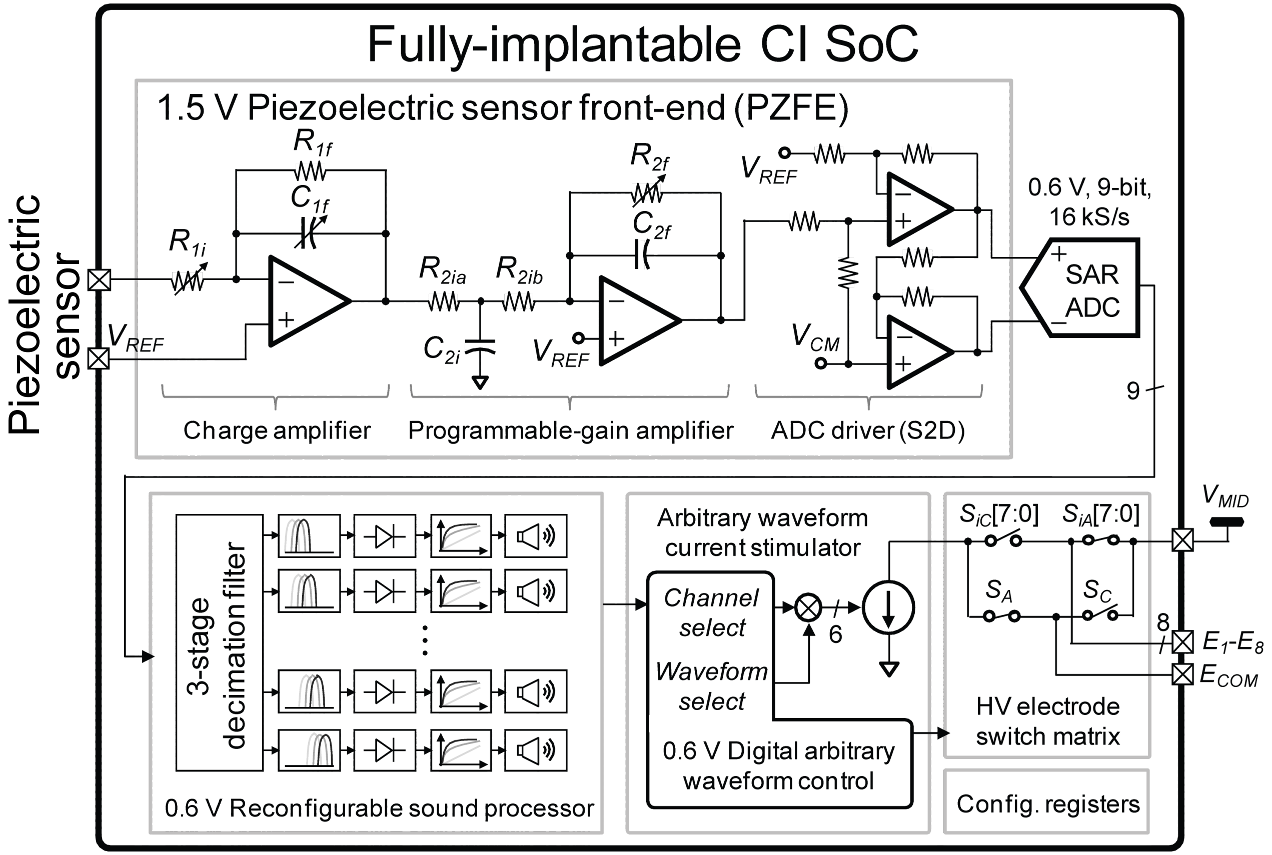


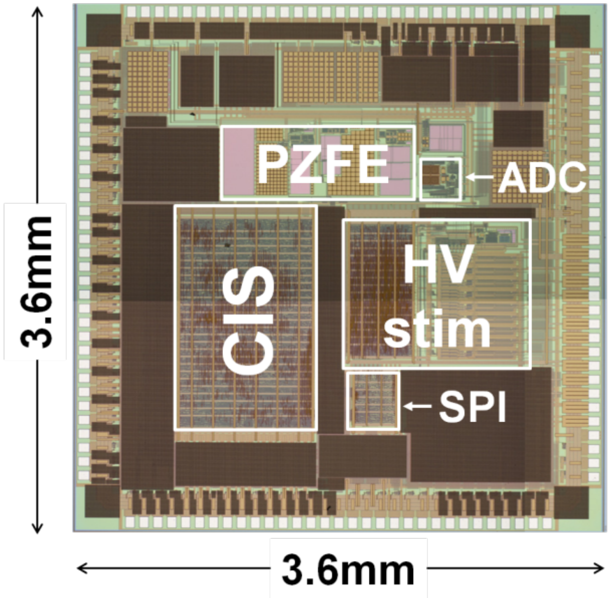
Limitations

- **Usage in shower/water sports**
- **Aesthetics and social stigma**

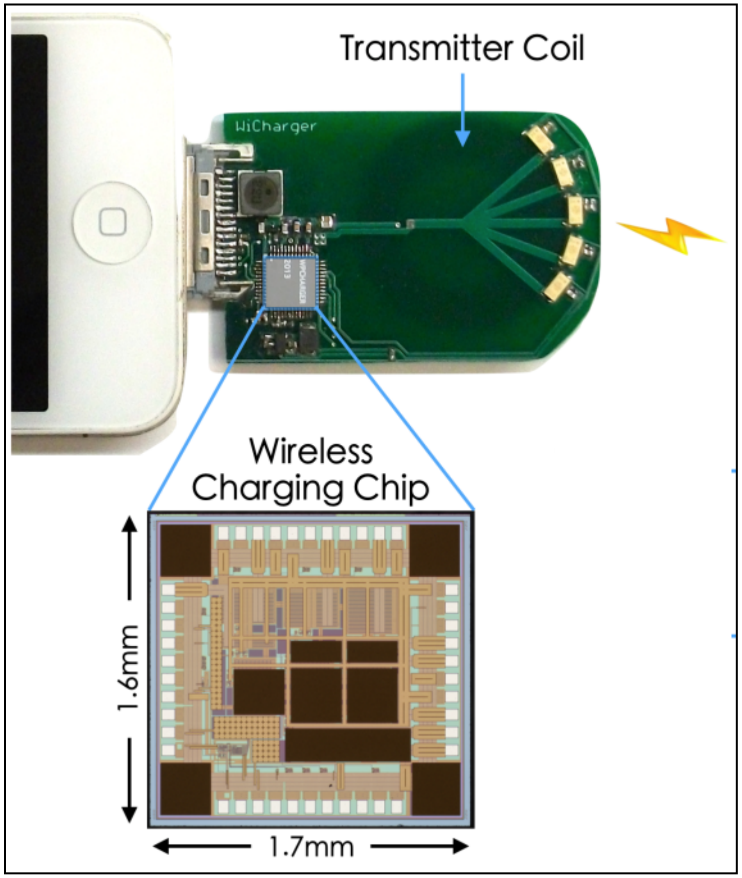
M. Yip, R.Jin, H. Nakajima, K. Stankovic, and A. P. Chandrakasan, "A Fully-Implantable Cochlear Implant SoC with Piezoelectric Middle-Ear Sensor and Energy-Efficient Stimulation in 0.18μm HVCMOS", ISSCC 2014

Prototype Implementation





Efficient Portable-to-Portable Wireless Charging



Wirelessly charge
low-power portables by
high-power portables

- Charge in 2 minutes for typical day use

Summary

- Energy efficiency achieved through :
  - Ultra-low-voltage operation
  - Hardwired architectures
  - Exploiting application attributes (e.g., data-driven processing)
  - Digital control of energy processing
  - Optimizing for short duty cycles
- Next generation sub-Hz optimized electronics will enable new energy harvesting applications

Exciting Opportunities Beyond Moore's Law Scaling